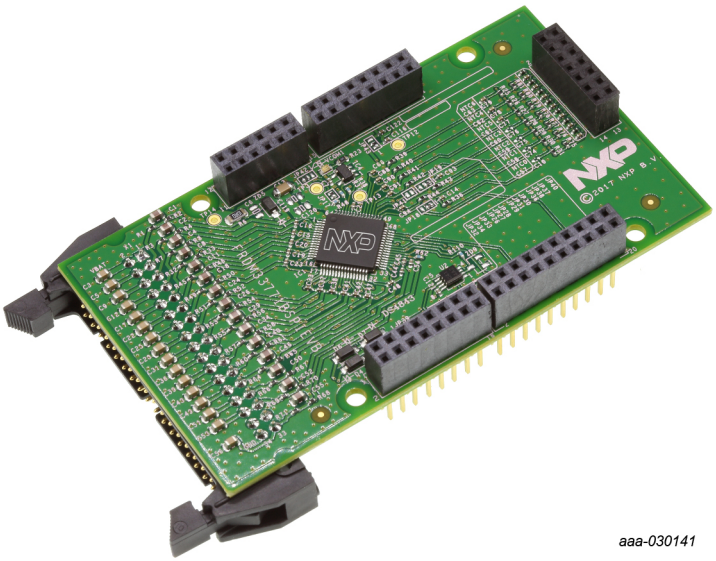
FRDM33771BSPIEVB

Featuring the MC33771B battery cell controller IC

Rev. 1.0 — 29 June 2018 User guide

1 FRDM33771BSPIEVB



aaa-030141

2 Important notice

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This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

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3 Getting started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. These development boards support a range of analog, mixed-signal, and power solutions. These boards incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

The tool summary page for FRDM33771BSPIEVB is at nxp.com/FRDM33771BSPIEVB. The overview tab on this page provides an overview of the device, a list of device features, a description of the kit contents, links to supported devices and a **Get Started** section.

The **Get Started** section provides information applicable to using the FRDM33771BSPIEVB.

1. Go to nxp.com/FRDM33771BSPIEVB.
2. On the **Overview** tab, locate the **Jump To** navigation feature on the left side of the window.
3. Select the **Get Started** link.
4. Review each entry in the **Get Started** section.
5. Download an entry by clicking on the linked title.

After reviewing the **Overview** tab, visit the other related tabs for additional information:

- **Documentation**: Download current documentation.
- **Software & Tools**: Download current hardware and software tools.
- **Buy/Parametrics**: Purchase the product and view the product parametrics.

After downloading files, review each file, including the user guide, which includes setup instructions. If applicable, the Bill of Materials (BOM), suporting schematics, and layout are available via NXP DocStore. [5]

3.1 Kit contents/packing list

The kit contents include:

- Assembled and tested evaluation board/module in anti-static bag
- Quick-start guide

3.2 Required equipment

To use this kit, you need:

- A 7- to 14-cell battery pack, such as BATT-14AAAPACK, or a battery pack emulator, such as BATT-14EMULATOR

4 Getting to know the hardware

4.1 Board overview

The FRDM33771BSPIEVB serves as a hardware evaluation tool in support of NXP's MC33771B device. The MC33771B is a battery cell controller that monitors up to 14 lithium-ion battery cells. It is designed for use in both automotive and industrial

applications. The device performs ADC conversion on the differential cell voltages and currents. It is also capable of battery charge coulomb counting and battery temperature measurements. The FRDM33771BSPIEVB is an ideal platform for rapid prototyping of MC33771B-based applications that involve current, voltage, and temperature sensing.

The FRDM33771BSPIEVB supports standard SPI interface. The information is digitally transmitted to a microcontroller for processing.

4.2 Board features

This FRDM33771BSPIEVB's main features are as follows:

- Standard SPI communication
- LED indicator for operation mode
- Cell-balancing resistors
- Cell sense input with RC filter
- GPIO: digital I/O, wake-up inputs, convert trigger inputs, ratiometric analog inputs, analog inputs with absolute measurements
- EEPROM (connected to the IC with I^2C interface) to store user-defined calibration parameters
- Fault detection pin report

4.3 Block diagram

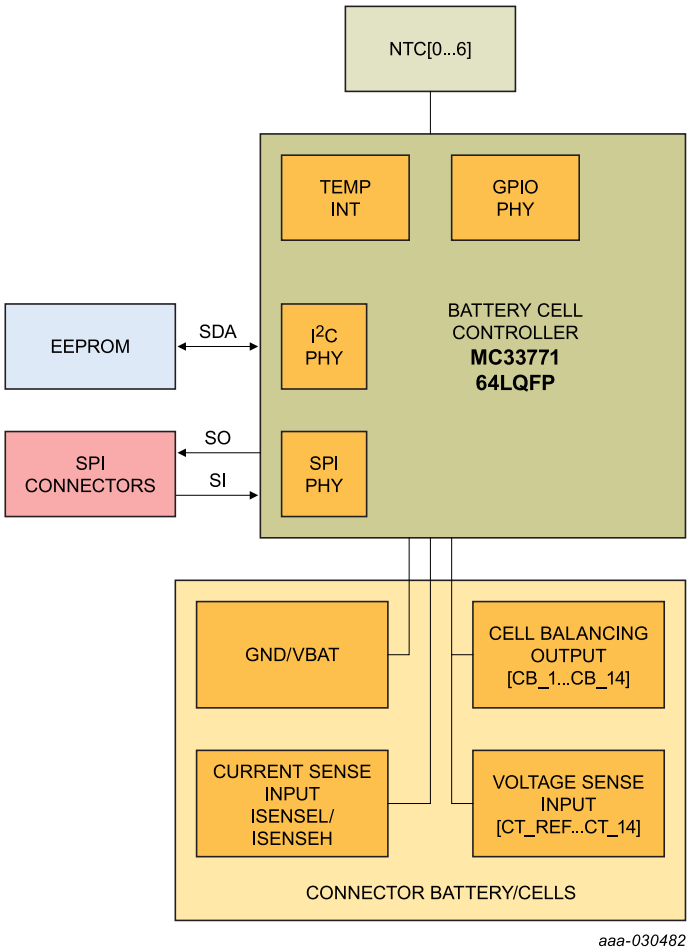

Figure 1. Block diagram

4.4 Device features

The MC33771B is a battery cell controller IC designed to monitor battery characteristics, such as voltage, current and temperature. The MC33771B contains all the circuit blocks necessary to perform synchronous battery cell voltage/current measurement, coulomb counting, cell temperature measurement and integrated cell balancing. The device supports the following functions:

Table 1. MC33771B device features

Device	Description	Features
MC33771B	Battery cell controller	• 9.6 V ≤ V_{PWR} ≤ 61.6 V operation, 75 V transient • 7 to 14 cells management • Isolated 2.0 Mbps differential communication or 4.0 Mbps SPI • Addressable on initialization • 0.8 mV maximum total voltage measurement error • Synchronized cell voltage/current measurement with coulomb count • Total stack voltage measurement • Seven GPIO/temperature sensor inputs • 5.0 V at 5.0 mA reference supply output • Automatic over/undervoltage and temperature detection routable to fault pin • Integrated sleep mode over/undervoltage and temperature monitoring • Onboard 300 mA passive cell balancing with diagnostics • Hot plug capable • Detection of internal and external faults, as open lines, shorts, and leakages • Designed to support ISO 26262, up to ASIL D safety capability • Fully compatible with the MC33772 for a maximum of six cells • Qualified in compliance with AECQ-100

4.5 Board description

The FRDM33771BSPIEVB allows the user to exercise all the functions of the MC33771B battery controller cell.

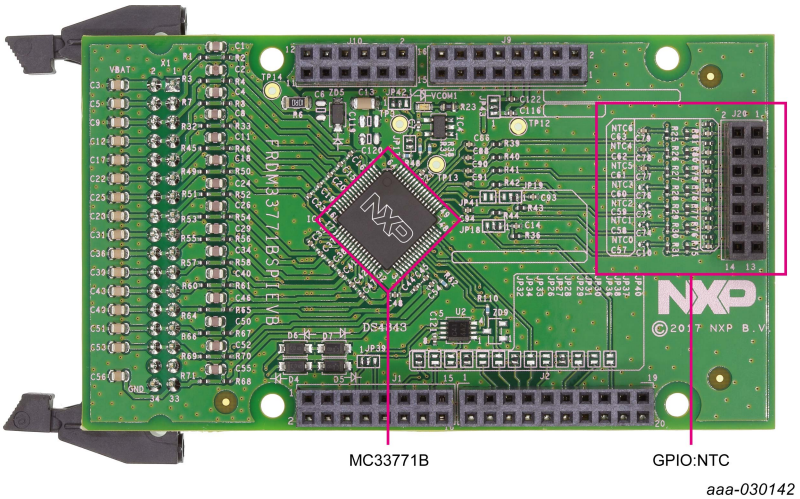

Figure 2. Board description

Table 2. Board description

Name	Description
MC33771B	Battery-cell controller IC
GPIO:NTC[0…6]	Support off-board NTC

4.6 VCOM LED

The VCOM LED is located on the board as shown in Figure 3.

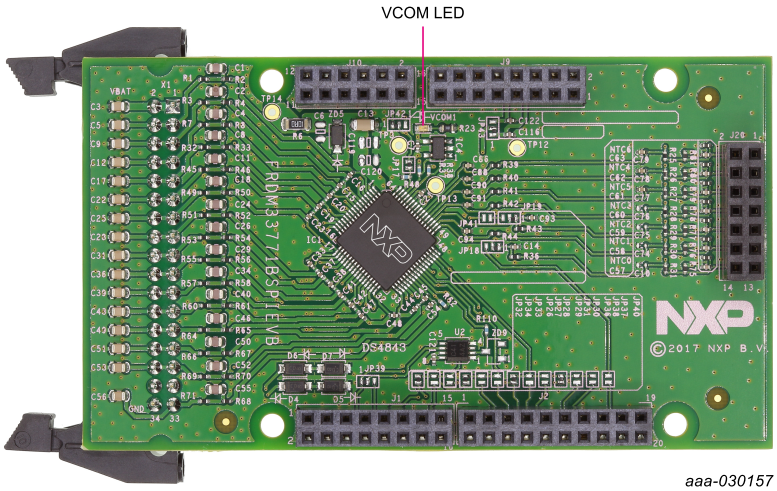

Figure 3. VCOM LED

The VCOM LED indicates when the device is in normal mode. Upon reset, the MC33771B enters into normal mode (VCOM turns on). If there is no activity on the bus after a timeout period of 60 seconds, the device enters low-power idle mode (VCOM turns off). Once the device is initialized, if no communication occurs on the TPL bus after one second, the device resets and the LED turns off (VCOM off). Depending on the device settings, the VCOM LED may flash 0.1...8 seconds during cyclic acquisition.

4.7 Test-point definitions

Figure 4 shows the location of the test points on the board.

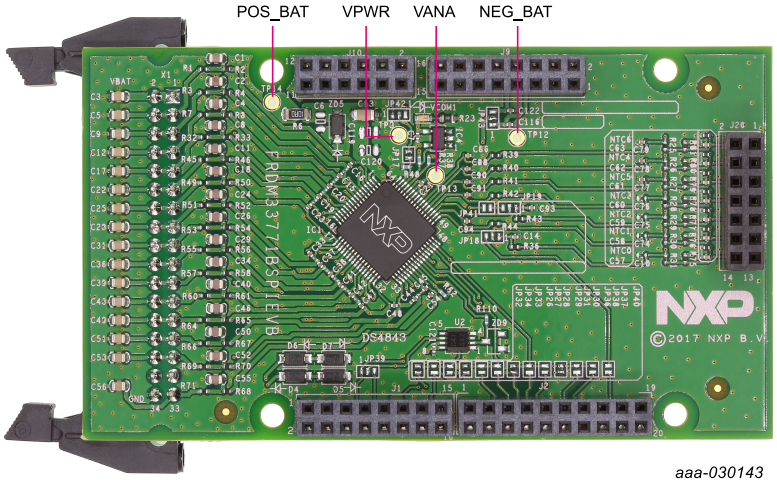

Figure 4. Test points

The following test points provide access to various signals to and from the board.

Table 3. Test points

Test-point name	Signal name	Description
NEG_BAT	GNDREF	Ground reference of the device
POS_BAT	V_{BAT}	Positive V_{BAT}
VPWR	VPWR	Power input to the device
VANA	VANA	Precision ADC analog supply output

4.8 Connectors

Figure 5 shows the location of connectors on the board. The following tables list the pinouts for each connector.

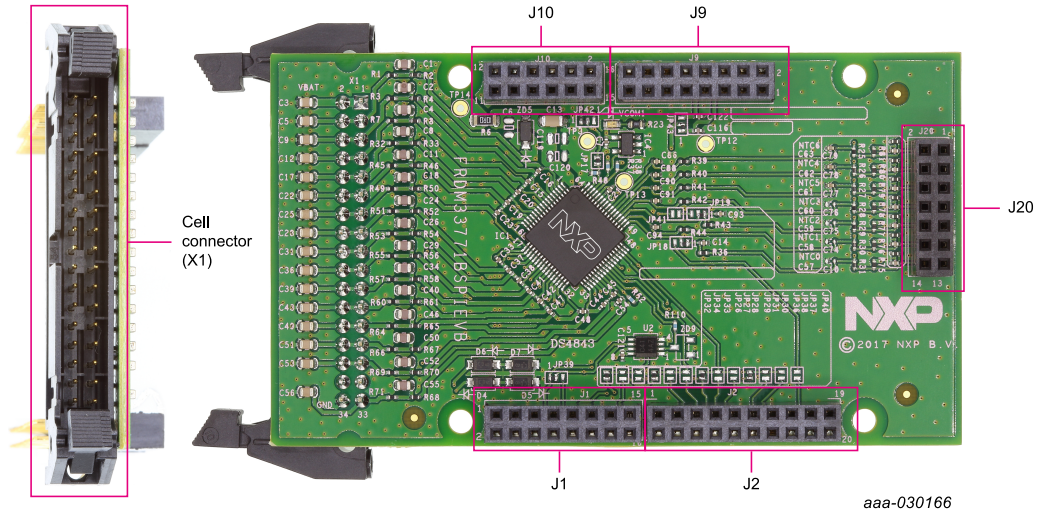

Figure 5. Connectors

Table 4. Connector (J1)

Pin #	Name	Description
6	FAULT_ALT0	Connected via J39_1-2 to FAULT_SPI_MCU
8	FAULT_ALT1	Connected via J39_3-2 to FAULT_SPI_MCU
9	SCLK_ALT0	Connected via J39 to SCLK
14	CSB_ALT0 and MISO_ ALT2	Connected via J26 to CSB and VIA J34 to SO
Other	—	No connection

Table 5. Connector (J2)

Pin #	Name	Description
5	CSB_ALT2	Connected via J28 to CSB
6	CSB_ALT1	Connected via J27 to CSB
7	MOSI_ALT2	Connected via J31 to SI

Pin #	Name	Description
8	MOSI_ALT0 and MISO_ ALT1	Connected via J29 to SI, J33 to SO
10	MISO_ALT0 and MOSI_ ALT1	Connected via J32 to SO, J30 to SI
11	SCLK_ALT2	Connected via J38 to SCLK
12	SCLK_ALT1	Connected via J37 to SCLK
14	GND	Connected to GND
18	GPIO0_WKU	Connected via J40 and J18_2-3 to GPIO0
Other	—	No connection

Table 6. Connector (J9)

Pin #	Name	Description
8	+3V3	+3.3 V supply
10	+5V_USB	+5 V USB supply
12	GND	Connected to GND
14	GND	Connected to GND
Other	—	No connection

Table 7. Connector (J10)

Pin #	Name	Description
2	RESET_ALT0	Connected via J42_1-2 and J19_2-3 to GPIO2
6	GPIO2_SOC	Connected via J41 to GPIO2_SOC
Other	—	No connection

Table 8. GPIO connector (J20)

Pin #	Name	Description
1	GND	To GND
2	NTC6_P	To GPIO6
3	GND	To GND
4	NTC5_P	To GPIO5
5	GND	To GND
6	NTC4_P	To GPIO4
7	GND	To GND
8	NTC3_P	To GPIO3
9	GND	To GND

Pin #	Name	Description
10	NTC2_P	To GPIO2
11	GND	To GND
12	NTC1_P	To GPIO1
13	GND	To GND
14	NTC0_P	To GPIO0

Table 9. Cell connector (X1)

Pin #	Connection	Description
X1-1 X1-2	VBAT	MC33771B Power supply
X1-3 X1-4	CT_14 CB_14	Cell pin 14 input with external LPF resistor. Cell balance driver. Terminate to cell 14 cell balance load resistor
X1-5 X1-6	CT_13 CB_14:13_C	Cell pin 13 input with external LPF resistor. Cell balance 14:13 common. Terminate to cell 14 and 13 common pin
X1-7 X1-8	CT_12 CB_13/CB_12	Cell pin 12 input with external LPF resistor. Cell balance driver. Terminate to cell 13 and 12 cell balance load resistor
X1-9 X1-10	CT_11 CB_12:11_C	Cell pin 11 input with external LPF resistor. Cell balance 12:11 common. Terminate to cell 12 and 11 common pin
X1-11 X1-12	CT_10 CB_11/CB_10	Cell pin 10 input with external LPF resistor. Cell balance driver. Terminate to cell 11 and 10 cell balance load resistor
X1-13 X1-14	CT_9 CB_10:9_C	Cell pin 9 input with external LPF resistor. Cell balance 10:9 common. Terminate to cell 10 and 9 common pin
X1-15 X1-16	CT_8 CB_9/CB_8	Cell pin 8 input with external LPF resistor. Cell balance driver. Terminate to cell 9 and 8 cell balance load resistor
X1-17 X1-18	CT_7 CB_8:7_C	Cell pin 7 input with external LPF resistor. Cell balance 8:7 common. Terminate to cell 8 and 7 common pin
X1-19 X1-20	CT_6 CB_7/CB_6	Cell pin 6 input with external LPF resistor. Cell balance driver. Terminate to cell 7 and 6 cell balance load resistor
X1-21 X1-22	CT_5 CB_6:5_C	Cell pin 5 input with external LPF resistor. Cell balance 6:5 common. Terminate to cell 6 and 5 common pin
X1-23 X1-24	CT_4 CB_5/CB_4	Cell pin 4 input with external LPF resistor. Cell balance driver. Terminate to cell 5 and 4 cell balance load resistor
X1-25 X1-26	CT_3 CB_4:3_C	Cell pin 3 input with external LPF resistor. Cell balance 4:3 common. Terminate to cell 4 and 3 common pin
X1-27 X1-28	CT_2 CB_3/CB_2	Cell pin 2 input with external LPF resistor. Cell balance driver. Terminate to cell 3 and 2 cell balance load resistor
X1-29 X1-30	CT_1 CB_2:1_C	Cell pin 1 input with external LPF resistor. Cell balance 2:1 common. Terminate to cell 2 and 1 common pin
X1-31	ISENSE_+	Current measurement input+ with external filter RC

Pin #	Connection	Description
X1-32	ISENSE_–	Current measurement input– with external filter RC
X1-33	CT_REF CB_1	Cell pin REF input with external LPF resistor. Cell balance driver. Terminate to cell 1 cell balance load resistor.
X1-34	GND	Negative_Battery

4.9 External EEPROM

The FRDM33771BSPIEVB has an integrated gateway communication link to an external local EEPROM. The MC33771B's I^2C Communication Interface manages communication with the EEPROM.

After a reset, the EEPROM is not enabled. When the EEPROM is enabled, the device can load the EEPROM calibration parameters into the MC33771B registers.

4.10 GPIO configuration

The FRDM33771BSPIEVB offers seven customizable GPIOs [GPIO_0...GPIO_6] for measuring external temperature with a bridge divider. [GPIO_0] can be used as the input for wake-up or fault daisy chain.

4.11 Cell terminal voltage measurement

The differential measurement of each cell terminal input is designed to function in conjunction with an external anti-aliasing filter with a corner frequency.

4.12 Current sensing

The FRDM33771BSPIEVB supports current sense function with off-board shunt resistor. The off-board shunt resistor shall be connected between X1-31 (ISENSE+) and X1-32 (ISENSE–). On-board current sensing filter and protection circuits can be found in EVB schematic shared via NXP DocStore (NDA required).

4.13 SPI communication interface

The MC33771B SPI interface is a standard SPI slave interface with a chip select (CSB), clock (SCLK), Slave Out (SO), and Slave In (SI). The SI/SO shifting of the data follows a first-in-first-out protocol, with both input and output words transferring the Most Significant Bit (MSB) first.

All SPI communication to the MC33771B is controlled by the microcontroller. One 40-bit register of previously requested data is retrieved through serial out for each current serial in message sent by the MCU. For message integrity and communication robustness, each SPI transmit message consists of six fields containing 40 bits.

The six transmit fields are defined as the following:

1. Cyclical redundancy check (8 bits)
2. Command field (4 bits)
3. Cluster ID field (4 bits)
4. Memory address field (7 bits)
5. Master/slave field (1 bit)

6. Memory data field (16 bits)

Messages having less or more than 40 bits or incorrect CRC are disregarded. Communication faults set the COM_ERR_FLT fault bit in the FAULT1_STATUS register and increments the COM_STATUS[COM_ERR_COUNT] register.

Detailed schematic, component selection, and layout recommendations can be obtained from the NXP DocStore (NDA required) [5].

5 Configuring the hardware

The FRDM33771BSPIEVB can be configured as a shield board connected to selected Freedom boards.

5.1 Compatible NXP MCU development platforms

FRDM33771BSPIEVB is compatible with multiple NXP MCU development platforms:

- FRDM-KL25Z (default)
- FRDM-KE06Z
- FRDM-KL43Z
- FRDM-KV31F
- FRDM-KW40Z
- FRDM-KEAZ128
- S32K144EVB
- Arduino R3

MCU development platform ordering, instruction, and other information is on nxp.com.

Table 10. Jumper setting to work with FRDM-KL25Z (default)

Jumper	Setting	Description
JP26	1-2	CSB
JP27	open	—
JP28	open	—
JP29	1-2	MOSI
JP30	open	—
JP31	open	—
JP32	1-2	MISO
JP33	open	—
JP34	open	—
JP36	1-2	SLCK
JP37	open	—
JP38	open	—
JP39	1-2	FAULT
JP42	1-2	RESET
JP43	1-2	3.3 V

Table 11. Jumper setting to work with FRDM-KE06Z

Jumper	Setting	Description
JP26	open	—
JP27	1-2	CSB
JP28	open	—
JP29	1-2	MOSI
JP30	open	—
JP31	open	—
JP32	open	—
JP33	open	—
JP34	1-2	MISO
JP36	open	—
JP37	1-2	SLCK
JP38	open	—
JP39	2-3	FAULT
JP42	2-3	RESET
JP43	1-2	3.3 V

Table 12. Jumper setting to work with FRDM-KL43Z

Jumper	Setting	Description
JP26	open	—
JP27	1-2	CSB
JP28	open	—
JP29	1-2	MOSI
JP30	open	—
JP31	open	—
JP32	1-2	MISO
JP33	open	—
JP34	open	—
JP36	open	—
JP37	1-2	SLCK
JP38	open	—
JP39	2-3	FAULT
JP42	2-3	RESET
JP43	1-2	3.3 V

Table 13. Jumper setting to work with FRDM-KV31F

Jumper	Setting	Description
JP26	open	—
JP27	1-2	CSB
JP28	open	—
JP29	1-2	MOSI
JP30	open	—
JP31	open	—
JP32	1-2	MISO
JP33	open	—
JP34	open	—
JP36	open	—
JP37	1-2	SLCK
JP38	open	—
JP39	2-3	FAULT
JP42	2-3	RESET
JP43	1-2	3.3 V

Table 14. Jumper setting to work with FRDM-KW40Z

Jumper	Setting	Description
JP26	1-2	CSB
JP27	open	—
JP28	open	—
JP29	open	—
JP30	1-2	MOSI
JP31	open	—
JP32	open	—
JP33	1-2	MISO
JP34	open	—
JP36	open	—
JP37	1-2	SLCK
JP38	open	—
JP39	2-3	FAULT
JP42	2-3	RESET
JP43	1-2	3.3 V

Table 15. Jumper setting to work with FRDM-KEAZ128

Jumper	Setting	Description
JP26	open	—
JP27	1-2	CSB
JP28	open	—
JP29	1-2	MOSI
JP30	open	—
JP31	open	—
JP32	1-2	MISO
JP33	open	—
JP34	open	—
JP36	open	—
JP37	1-2	SLCK
JP38	open	—
JP39	1-2	FAULT
JP42	1-2	RESET
JP43	1-2	3.3 V

Table 16. Jumper setting to work with S32K144EVB

Jumper	Setting	Description
JP26	open	—
JP27	1-2	CSB
JP28	open	—
JP29	1-2	MOSI
JP30	open	—
JP31	open	—
JP32	1-2	MISO
JP33	open	—
JP34	open	—
JP36	open	—
JP37	1-2	SLCK
JP38	open	—
JP39	2-3	FAULT
JP42	1-2	RESET
JP43	2-3	5 V

Table 17. Jumper setting to work with Arduino R3

Arduino R3 has a single-line connector that connects to the outer row of the FRDM33771BSPIEVB connectors.

Jumper	Setting	Description
JP26	open	—
JP27	1-2	CSB
JP28	open	—
JP29	1-2	MOSI
JP30	open	—
JP31	open	—
JP32	1-2	MISO
JP33	open	—
JP34	open	—
JP36	open	—
JP37	1-2	SLCK
JP38	open	—
JP39	2-3	FAULT
JP42	2-3	RESET
JP43	1-2	3.3 V

5.2 Freedom board configuration

The layout of the connectors allow MCU development boards mentioned in Section 5.1 "Compatible NXP MCU development platforms" to be mounted directly to the FRDM33771BSPIEVB. See Figure 6. When both boards are connected together, the SPI connector is directly connected with the MCU SPI pins. The routing of SPI signals through the Arduino connectors depends on the specific Freedom board being used. In this configuration, power is supplied to the FRDM33771BSPIEVB through a USB cable connected between the Freedom board and a PC. No external power supply is required.

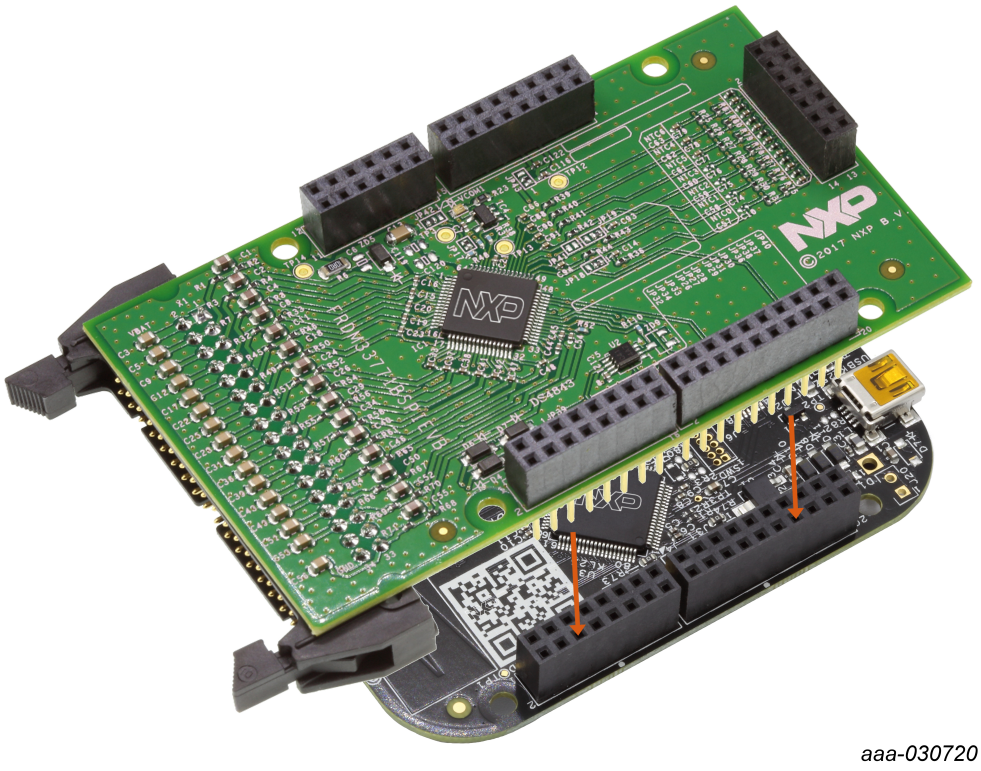

Figure 6. FRDM33771BSPIEVB mounted to a FRDM-KL25Z

The board must be modified to be compatible with each specific Freedom board. This modification is described in Section 5.1 "Compatible NXP MCU development platforms".

5.3 Off-board NTC configuration

FRDM33771BSPIEVB supports off-board NTC, please follow the instruction in the following table.

Table 18. Off-board NTC configuration

Remove	Connect off-board NTC between
NTC0	J20 13-14
NTC1	J20 11-13
NTC2	J20 9-10
NTC3	J20 7-8
NTC4	J20 5-6
NTC5	J20 3-4
NTC6	J20 1-2

6 Available accessories

Note: *NXP does not assume liability, endorse, or warrant components from external manufacturers are referenced in circuit drawings or tables. While NXP offers component*

recommendations in this configuration, it is the customer's responsibility to validate their application.

Table 19. Bill of materials

Part number	Description
M50-9101742	34-pin ribbon cable
BATT-14AAAPACK	3- to 14-cell configurable AAA battery pack
BATT-14EMULATOR	14-cell slider battery pack emulator kit with shunt for current sense

7 References

[1] **Board summary page** — nxp.com/FRDM33771BSPIEVB

[2] **Product summary page** — nxp.com/BATTERY-CELL-CONTROLLERS

[3] **Tool summary page for BATT-14AAAPACK battery pack** — nxp.com/BATT-14AAAPACK

[4] **Tool summary page for battery emulators** — nxp.com/BATT-14EMULATOR

[5] **NXP DocStore** — docstore.nxp.com

8 Revision history

Table 20. Revision history

Rev	Date	Description
v.1.0	20180629	Initial release

9 Legal information

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Date of release: 29 June 2018
Document identifier: FRDM33771BSPIEVBUG