

**OptiMOS™ 3 M-Series Power-MOSFET**
**Features**

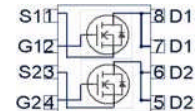
- Dual N-channel
- Optimized for 5V driver application (Notebook, VGA, POL)
- Low FOM<sub>SW</sub> for High Frequency SMPS
- 100% Avalanche tested
- Very low on-resistance  $R_{DS(on)}$  @  $V_{GS}=4.5\text{ V}$
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Qualified for consumer level application
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21


**Product Summary**

$V_{DS}$		30	V
$R_{DS(on),max}$	$V_{GS}=10\text{ V}$	15	mΩ
	$V_{GS}=4.5\text{ V}$	18.2	
$I_D$		9.3	A

**PG-DSO-8**


Type	Package	Marking
BSO150N03MD G	PG-DSO-8	150N03MD


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value		Unit
			10 secs	steady state	
Continuous drain current <sup>1)</sup>	$I_D$	$V_{GS}=10\text{ V}, T_A=25\text{ °C}$	9.3	8	A
		$V_{GS}=10\text{ V}, T_A=90\text{ °C}$	6.4	5.4	
		$V_{GS}=4.5\text{ V}, T_A=25\text{ °C}$	8.4	7	
		$V_{GS}=4.5\text{ V}, T_A=90\text{ °C}$	5.8	4.9	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_A=25\text{ °C}$	65		
Avalanche current, single pulse <sup>3)</sup>	$I_{AS}$	$T_A=25\text{ °C}$	9.3		
Avalanche energy, single pulse	$E_{AS}$	$I_D=9.3\text{ A}, R_{GS}=25\text{ Ω}$	20		mJ
Gate source voltage	$V_{GS}$		±20		V
Power dissipation <sup>1)</sup>	$P_{tot}$	$T_A=25\text{ °C}$	2	1.4	W
Operating and storage temperature	$T_j, T_{stg}$		-55 ... 150		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics**

Thermal resistance, junction - soldering point	$R_{thJS}$		-	-	50	K/W
Thermal resistance, junction - ambient	$R_{thJA}$	minimal footprint, $t_p \leq 10$ s	-	-	110	
		minimal footprint, steady state	-	-	150	
		6 cm <sup>2</sup> cooling area <sup>1)</sup> , $t_p \leq 10$ s	-	-	62.5	
		6 cm <sup>2</sup> cooling area <sup>1)</sup> , steady state	-	-	90	

**Electrical characteristics, at  $T_j=25$  °C, unless otherwise specified**
**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0$ V, $I_D=1$ mA	30	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}$ , $I_D=250$ $\mu$ A	1	-	2	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=30$ V, $V_{GS}=0$ V, $T_j=25$ °C	-	0.1	10	$\mu$ A
		$V_{DS}=30$ V, $V_{GS}=0$ V, $T_j=125$ °C	-	10	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=16$ V, $V_{DS}=0$ V	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5$ V, $I_D=8.4$ A	-	14.6	18.2	m $\Omega$
		$V_{GS}=10$ V, $I_D=9.3$ A	-	12.5	15	
Gate resistance	$R_G$		0.5	1.1	1.9	$\Omega$
Transconductance	$g_{fs}$	$ V_{DS}  > 2 I_D  R_{DS(on)max}$ , $I_D=9.3$ A	12	24	-	S

<sup>1)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70  $\mu$ m thick) copper area for drain connection. PCB is vertical in still air. One transistor active.

<sup>2)</sup> See figure 3 for more detailed information

<sup>3)</sup> See figure 13 for more detailed information

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=15\text{ V},$ $f=1\text{ MHz}$	-	970	1300	pF
Output capacitance	$C_{oss}$		-	340	450	
Reverse transfer capacitance	$C_{rss}$		-	20	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=15\text{ V}, V_{GS}=4.5\text{ V},$ $I_D=9.3\text{ A}, R_G=1.6\ \Omega$	-	7.3	-	ns
Rise time	$t_r$		-	3.8	-	
Turn-off delay time	$t_{d(off)}$		-	8.7	-	
Fall time	$t_f$		-	4.2	-	

**Gate Charge Characteristics<sup>4)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=15\text{ V}, I_D=9.3\text{ A},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	2.8	-	nC
Gate charge at threshold	$Q_{g(th)}$		-	1.5	-	
Gate to drain charge	$Q_{gd}$		-	1.4	-	
Switching charge	$Q_{sw}$		-	2.6	-	
Gate charge total	$Q_g$		-	6.1	8	
Gate plateau voltage	$V_{plateau}$		-	2.9	-	
Gate charge total	$Q_g$	$V_{DD}=15\text{ V}, I_D=9.3\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	12.6	17	nC
Gate charge total, sync. FET	$Q_{g(sync)}$	$V_{DS}=0.1\text{ V},$ $V_{GS}=0\text{ to }4.5\text{ V}$	-	5.3	7.0	
Output charge	$Q_{oss}$	$V_{DD}=15\text{ V}, V_{GS}=0\text{ V}$	-	8.9	12	

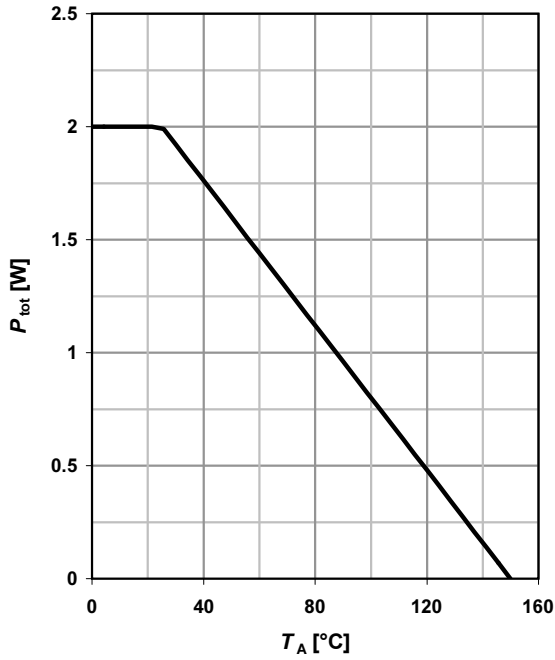
**Reverse Diode**

Diode continuous forward current	$I_S$	$T_A=25\text{ }^\circ\text{C}$	-	-	2.4	A
Diode pulse current	$I_{S,pulse}$		-	-	65	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=9.3\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.87	1.1	V
Reverse recovery charge	$Q_{rr}$	$V_R=15\text{ V}, I_F=I_S,$ $di_F/dt=400\text{ A}/\mu\text{s}$	-	-	10	nC

<sup>4)</sup> See figure 16 for gate charge parameter definition

**1 Power dissipation**

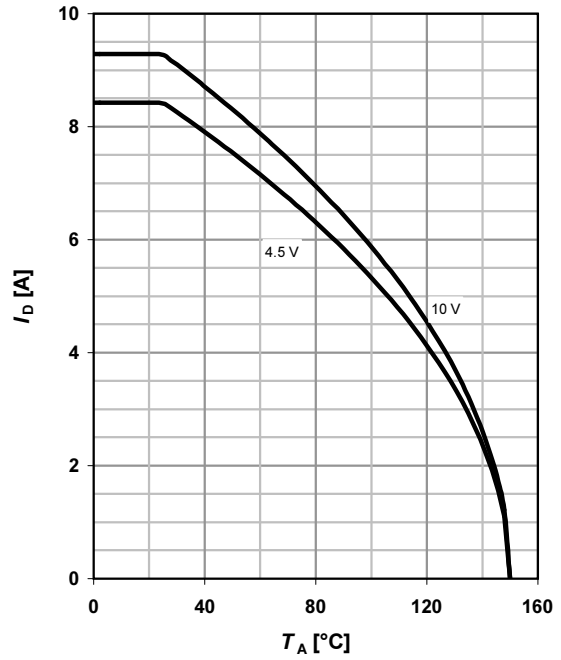
$P_{tot}=f(T_A); t_p \leq 10 \text{ s}$



**2 Drain current**

$I_D=f(T_A); t_p \leq 10 \text{ s}$

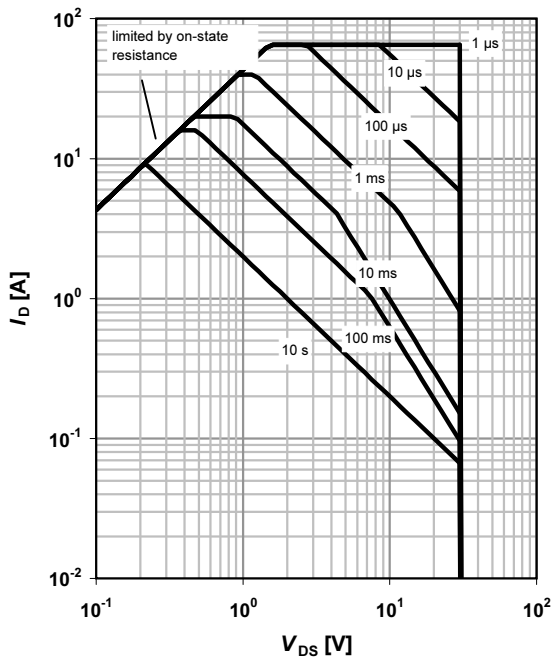
parameter:  $V_{GS}$



**3 Safe operating area**

$I_D=f(V_{DS}); T_A=25 \text{ °C}^2; D=0$

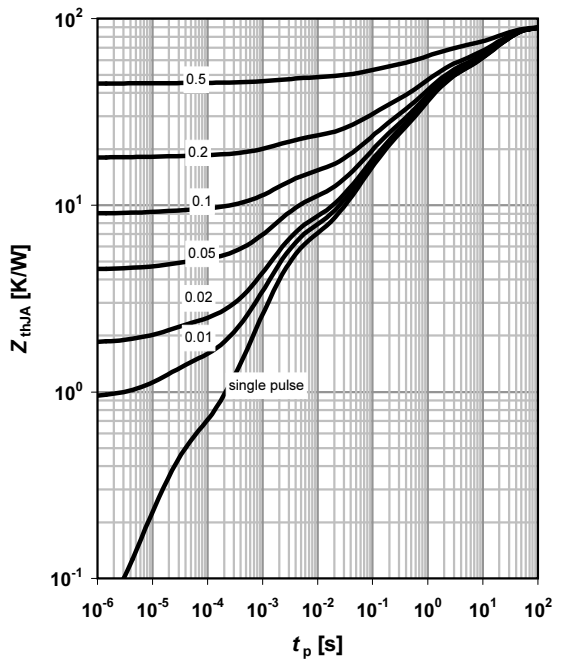
parameter:  $t_p$



**4 Max. transient thermal impedance**

$Z_{thJA}=f(t_p)^2$

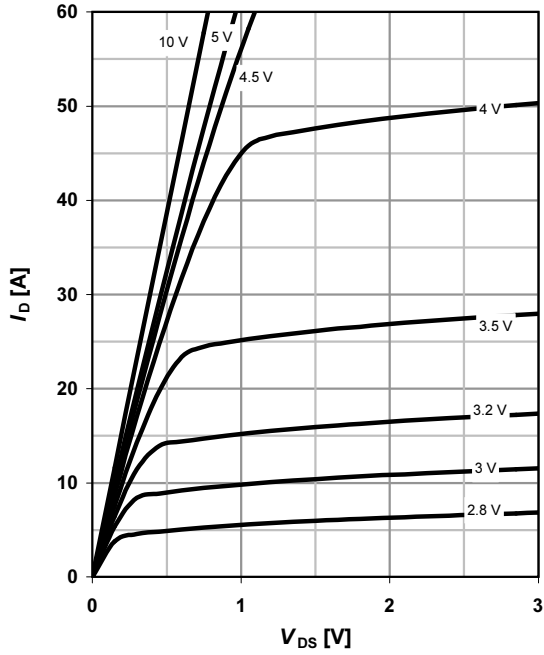
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

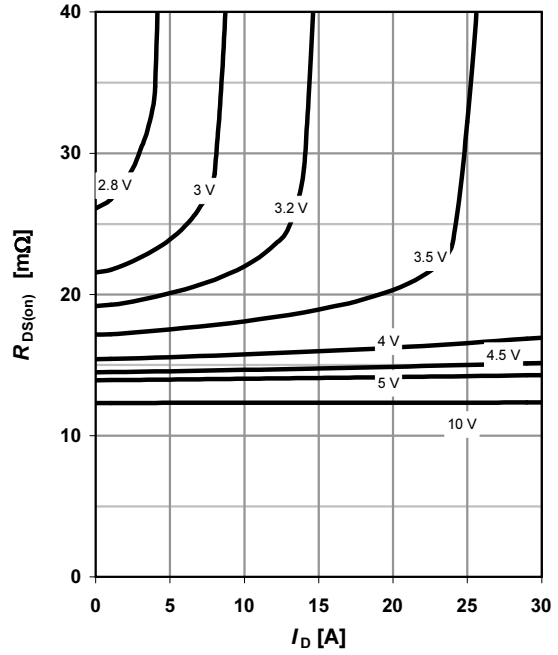
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

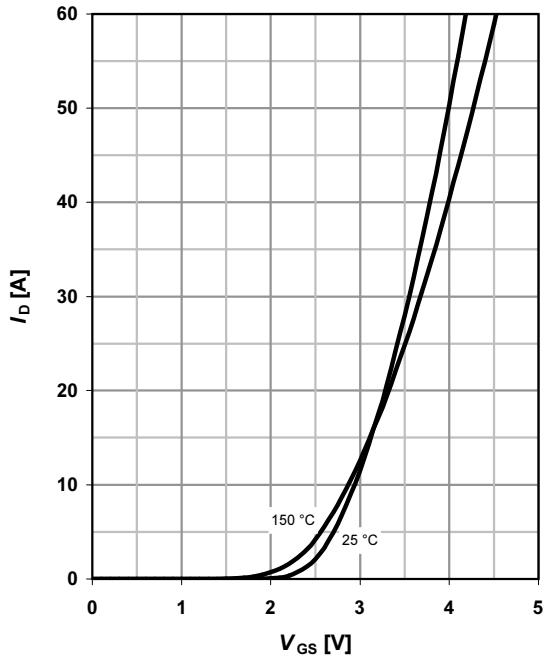
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

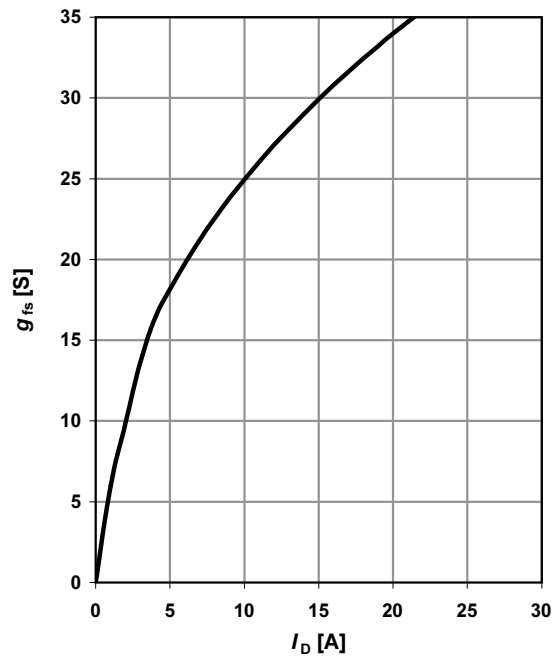
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



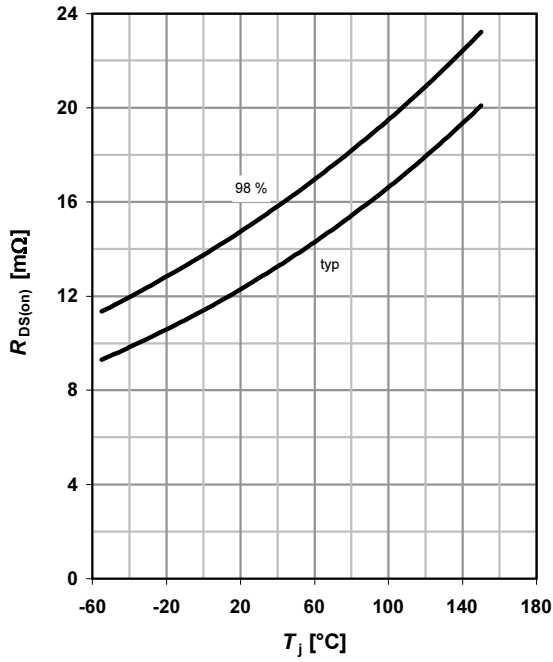
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



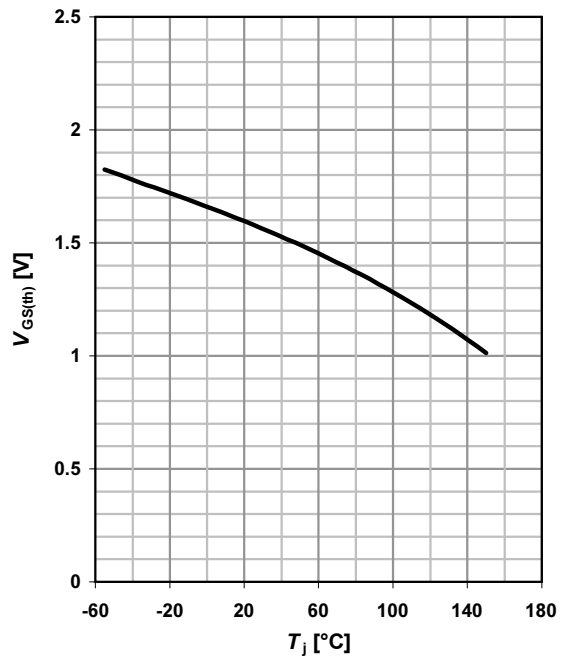
**9 Drain-source on-state resistance**

$R_{DS(on)} = f(T_j); I_D = 9.3 \text{ A}; V_{GS} = 10 \text{ V}$



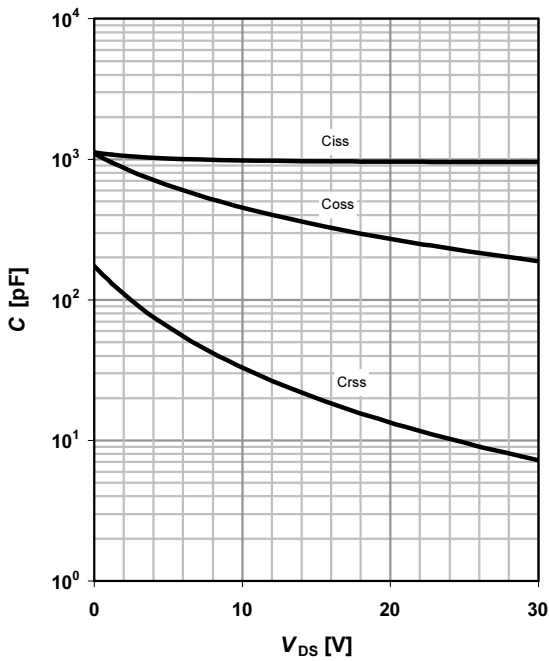
**10 Typ. gate threshold voltage**

$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}; I_D = 250 \mu\text{A}$



**11 Typ. capacitances**

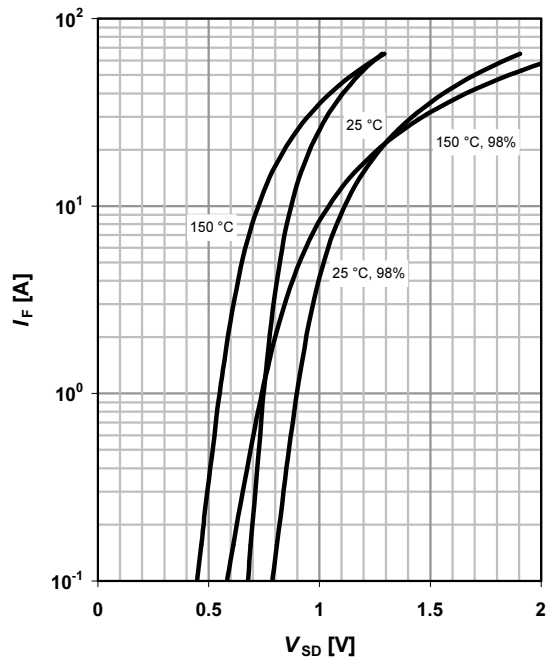
$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F = f(V_{SD})$

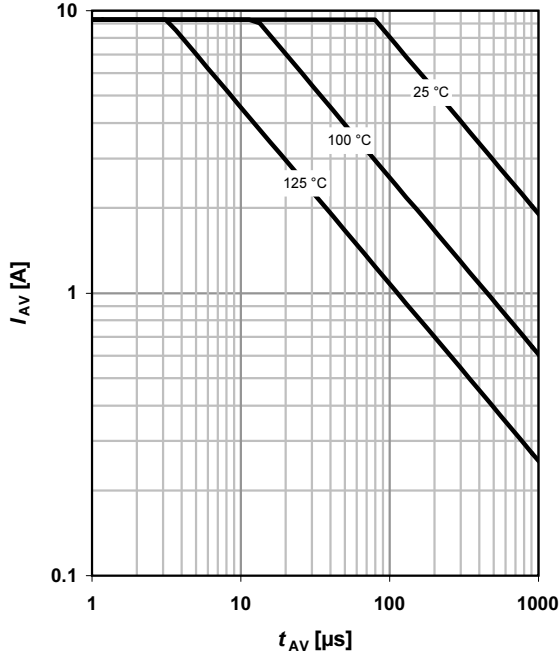
parameter:  $T_j$



**13 Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

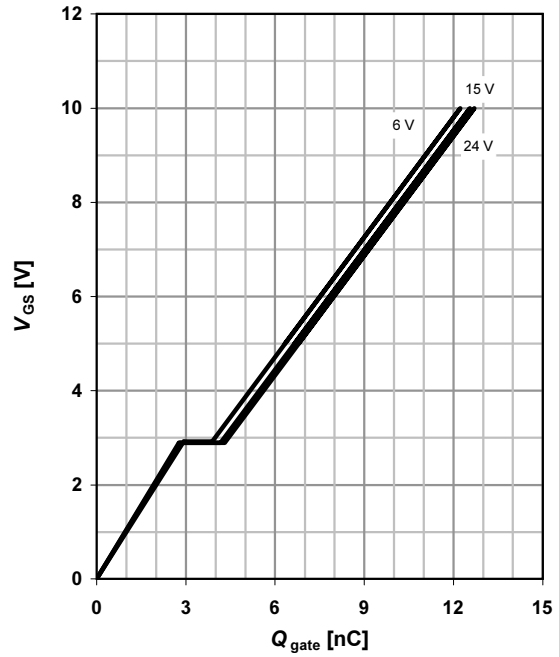
parameter:  $T_{j(start)}$



**14 Typ. gate charge**

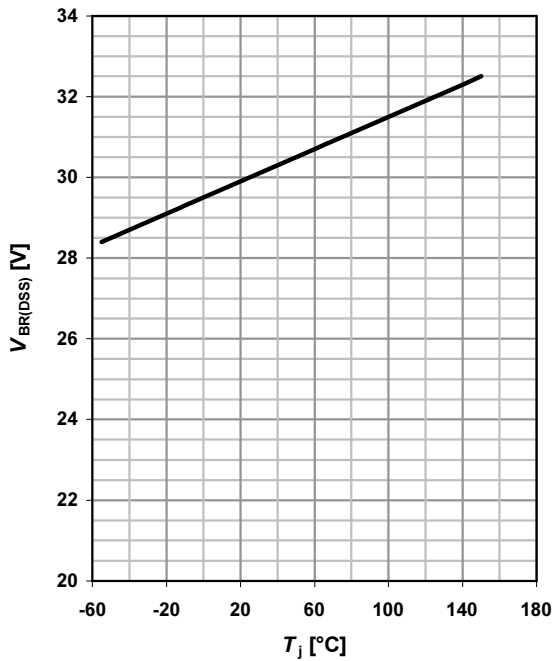
$V_{GS}=f(Q_{gate}); I_D=9.3 \text{ A pulsed}$

parameter:  $V_{DD}$

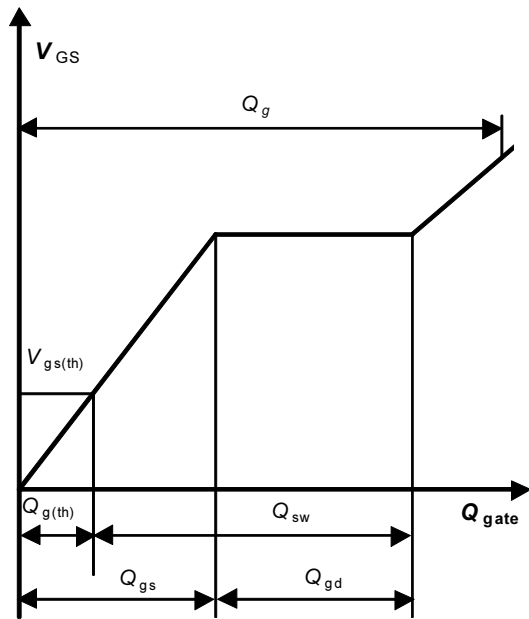


**15 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$

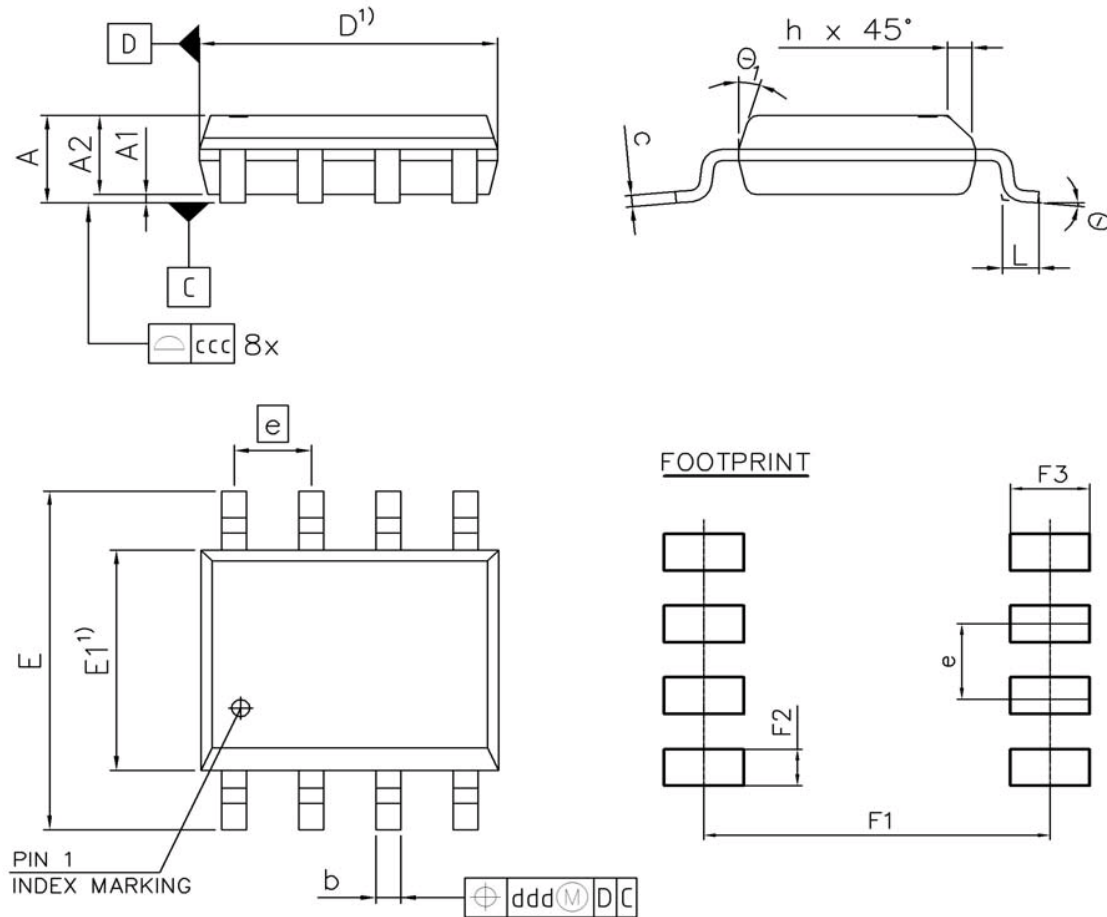


**16 Gate charge waveforms**



Package Outline

PG-DSO-8: Outline



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	1.75	-	0.069
A1	0.10	-	0.004	-
A2	1.25	1.65	0.049	0.065
b	0.35	0.51	0.014	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27		0.050	
N	8		8	
L	0.39	0.89	0.015	0.035
h	0.23	0.50	0.009	0.020
$\Theta$	0°	8°	0°	8°
$\Theta_1$	-	19°	-	19°
ccc	0.10		0.004	
ddd	0.25		0.010	
F1	5.59	5.79	0.220	0.228
F2	0.55	0.75	0.022	0.030
F3	1.21	1.41	0.048	0.056

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