



SANYO Semiconductors

DATA SHEET

An ON Semiconductor Company

Monolithic Linear IC

LA72715NV

JPN MTS (Multi Channel Television Sound) Decoder IC

Overview

JPN MTS (Multi Channel Television Sound) Decoder IC

Features

- With SIF circuit, alignment-free* STEREO channel separation.
* In base band signal input mode, separation is adjusted by input level.
- Three I²C slave-addresses are prepared.
- The maximum output level is as large as 4.2dBV.
(Frequency = 1kHz, distortion = less than 3%, V_{CC} = 5V, TYP)
- The external clock is unnecessary.
- A couple of external input terminal is prepared.

Functions

- Stereo & Bilingual demodulation.
- Stereo & Bilingual detection.
- Just clock out.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum power supply voltage	V _{CCH} max		7.0	V
Allowable power dissipation	Pd max	Ta ≤ 80°C, Mounted on a specified board*	203	mW
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-55 to +150	°C

* Mounted on a specified board: 114.3mm × 76.1mm × 1.6mm glass epoxy board

■ Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our customer shall be solely responsible for the use.

■ Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

SANYO Semiconductor Co.,Ltd.

<http://semicon.sanyo.com/en/network>

LA72715NV

Operating Ranges at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Recommended operating voltage	V _{CCH}		5.0	V
Allowable operating voltage	V _{CCH op}		4.5 to 5.5	V

Electrical Characteristics at Ta = 25°C, V_{DD} = 5V

[Condition of input signal at pin 5]

BASE BAND input

[Output] L-ch: pin 18, R-ch: pin 17

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Current dissipation	I _{CC1}	No signal, Inflow current at pin 19	18	26	34	mA
MONO output level	V _{OMN1}	fm = 1kHz, 100% Mod, Pre-emphasis OFF	-6	-4.5	-3	dBV
			501	595	708	mVrms
MONO L/R level difference	ΔV _{OMN1}	fm = 1kHz, 100% Mod, Pre-emphasis OFF	-1	0	1	dB
MONO distortion	THDM1	fm = 1kHz, 100% Mod, Pre-emphasis OFF		0.2	0.5	%
MONO frequency characteristics	FCM1	fm = 10kHz/1kHz, 100% Mod, 15kHz LPF Pre-emphasis OFF	-18	-13.5		dB
MONO S/N	SNM1	Non Mod, 15kHz LPF	60	65		dB
STEREO output level	V _{OST1}	fm = 1kHz, 100% Mod, Cue (Stereo), 15kHz LPF	-6	-4.5	-3	dBV
			501	595	708	mVrms
STEREO distortion	THDS1	fm = 1kHz, 100% Mod, Cue (Stereo), 15kHz LPF		0.5	1	%
STEREO S/N	SNS1	Sub Carrier (Non Mod), Cue (Stereo), 15kHz LPF	50	60		dB
Main output level	V _{OMA1}	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF	-6	-4.5	-3	dBV
			501	595	708	mVrms
Main distortion	THDMA1	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF		0.2	0.5	%
Main S/N	SNMA1	Sub Carrier (Non Mod), Cue (Bilingual), 15kHz LPF	60	65		dB
SUB output level	V _{SU1}	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF	-6	-4.5	-3	dBV
			501	595	708	mVrms
SUB distortion	THDSU1	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF		0.7	1.5	%
SUB frequency characteristics	FCSU1	fm = 10kHz/1kHz, 60% Mod, Cue (Bilingual), 15kHz LPF, Pre-emphasis OFF	-18	-14.5		dB
SUB Main S/N	SNSU1	Sub Carrier (Non Mod), Cue (Bilingual), 15kHz LPF	50	60		dB
STEREO separation L → R	SEPR1	fm = 1kHz (L-only), 60% Mod, Cue (Stereo), 15kHz LPF	35	43		dB
STEREO separation R → L	SEPL1	fm = 1kHz (R-only), 60% Mod, Cue (Stereo), 15kHz LPF	35	43		dB
Stay behind carrier level (SUB)	CLSU1	Main = 0%, Sub = 0% (Carrier) Cue (Bilingual)		-50	-40	dBV
Stay behind carrier level (MAIN)	CLMA1	Main = 0%, Sub = 0% (Carrier) Cue (Bilingual)		-55	-45	dBV
Cross-talk MAIN → SUB	CTSUB1	Main : fm = 1kHz, 100% modulation, Cue (Bilingual), 1kHz BPF	55	62		dB
Cross-talk SUB → MAIN	CTMA1	Sub : fm = 1kHz, 100% modulation, Cue (Bilingual), 1kHz BPF	55	62		dB
MODE output MONO	MODMO1	Input = Mono Signal	1.7	2	2.3	V
MODE output STEREO	MODST1	Input = Stereo Signal	0	1	1.3	V
MODE output BILINGUAL	MODBI1	Input = Bilingual Signal	2.7	3	3.3	V
Just Clock output High voltage	JCH1	f = 400Hz (mono), 25% Mod	4			V
Just Clock output Low voltage	JCL1	f = 400Hz (mono), 10% Mod			1	V
Max Output level	MOL1	f = 1kHz, distortion = 3%	3.3	4.2		dBV
			1462	1622		mVrms

Continued on next page.

LA72715NV

Continued from preceding page.

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
EXTERNAL input level	EXTIN1	f = 1kHz, (pin 12 & pin 13 input)		-14.5		dBV
				188.4		mVrms
8pin-CONTROL "H"	MUTEH	MUTE-ON	3.0		V _{CC}	V
8pin-CONTROL "OPEN"	MUTEOP	MUTE-OFF		0.9		V
8pin-CONTROL "L"	MUTEL	MUTE-OFF & Detection AREA CONROL	0		0.2	V

[Condition of input signal at pin 5]

Deviation of SIF input MONO : (fm = 1kHz) 100%→4.5MHz±25kHz Pre-Emphasis ON

[Output] L-ch : pin 18, R-ch : pin 17

Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Current dissipation	I _{CC2}	No signal, Inflow current at pin 19	20	28	36	mA
Input sensitivity level	V _{SIN}	fc = 4.5MHz	70	90	110	dBμV
			3.16	31.62	316.2	mVrms
MONO output level	V _{OMN2}	fm = 1kHz, 100% Mod, Pre-emphasis OFF	-6	-4.5	-3	dBV
			501	595	708	mVrms
MONO L/R level difference	ΔV _{OMN2}	fm = 1kHz, 100% Mod, Pre-emphasis OFF	-1	0	1	dB
MONO distortion	THDM2	fm = 1kHz, 100% Mod, Pre-emphasis OFF		0.2	0.5	%
MONO frequency characteristics	FCM2	fm = 10kHz/1kHz, 100% Mod, 15kHz LPF Pre-emphasis OFF	-18	-13.5		dB
MONO S/N	SNM2	Non Mod, 15kHz LPF	55	60		dB
STEREO output level	V _{OST2}	fm = 1kHz, 100% Mod, Cue (Stereo), 15kHz LPF	-6	-4.5	-3	dBV
			501	595	708	mVrms
STEREO distortion	THDS2	fm = 1kHz, 100% Mod, Cue (Stereo), 15kHz LPF		0.5	1	%
STEREO S/N	SNS2	Sub Carrier (Non Mod), Cue (Stereo), 15kHz LPF	50	57		dB
Main output level	V _{OMA2}	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF	-6	-4.5	-3	dBV
			501	595	708	mVrms
Main distortion	THDMA2	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF		0.2	0.5	%
Main S/N	SNMA2	Sub Carrier (Non Mod), Cue (Bilingual), 15kHz LPF	55	60		dB
SUB output level	V _{OSU2}	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF	-6	-4.5	-3	dBV
			501	595	708	mVrms
SUB distortion	THDSU2	fm = 1kHz, 100% Mod, Cue (Bilingual), 15kHz LPF		0.7	1.5	%
SUB frequency characteristics	FCSU2	fm = 10kHz/1kHz, 60% Mod, Cue (Bilingual), 15kHz LPF, Pre-emphasis OFF	-18	-14.5		dB
SUB Main S/N	SNSU2	Sub Carrier (Non Mod), Cue (Bilingual), 15kHz LPF	50	58		dB
STEREO separation L → R	SEPR2	fm = 1kHz (L-only), 60% Mod, Cue (Stereo), 15kHz LPF	35	38		dB
STEREO separation R → L	SEPL2	fm = 1kHz (R-only), 60% Mod, Cue (Stereo), 15kHz LPF	35	38		dB
Stay behind carrier level (SUB)	CLSU2	Main = 0%, Sub = 0% (Carrier) Cue (Bilingual)		-50	-40	dBV
Stay behind carrier level (MAIN)	CLMA2	Main = 0%, Sub = 0% (Carrier) Cue (Bilingual)		-55	-45	dBV
Cross-talk MAIN → SUB	CTSUB2	Main : fm = 1kHz, 100% modulation, Cue (Bilingual), 1kHz BPF	55	62		dB
Cross-talk SUB → MAIN	CTMA2	Sub : fm = 1kHz, 100% modulation, Cue (Bilingual), 1kHz BPF	55	62		dB
MODE output MONO	MODMO2	Input = Mono Signal	1.7	2	2.3	V
MODE output STEREO	MODST2	Input = Stereo Signal	0	1	1.3	V
MODE output BILINGUAL	MODBI2	Input = Bilingual Signal	2.7	3	3.3	V
Just Clock output High voltage	JCH2	f = 400Hz (mono), 25%Mod	4			V

Continued on next page.

LA72715NV

Continued from preceding page.

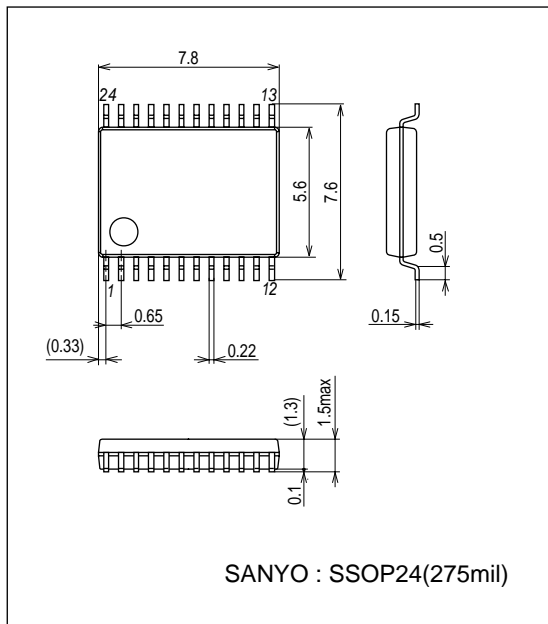
Parameter	Symbol	Conditions	Ratings			unit
			min	typ	max	
Just Clock output Low voltage	JCL2	f = 400Hz (mono), 10%Mod			1	V
Max Output level	MOL2	f = 1kHz, distortion = 3%	3.3	4.2		dBV
			1462	1622		mVrms
EXTERNAL input level	EXTIN2	f = 1kHz, (pin 12 & pin 13 input)		-14.5		dBV
				188.4		mVrms
8pin-CONTROL "H"	MUTEH	MUTE-ON	3.0		V _{CC}	V
8pin-CONTROL "OPEN"	MUTEOP	MUTE-OFF		0.9		V
8pin-CONTROL "L"	MUTEL	MUTE-OFF & Detection AREA CONROL	0		0.2	V

Package Dimensions

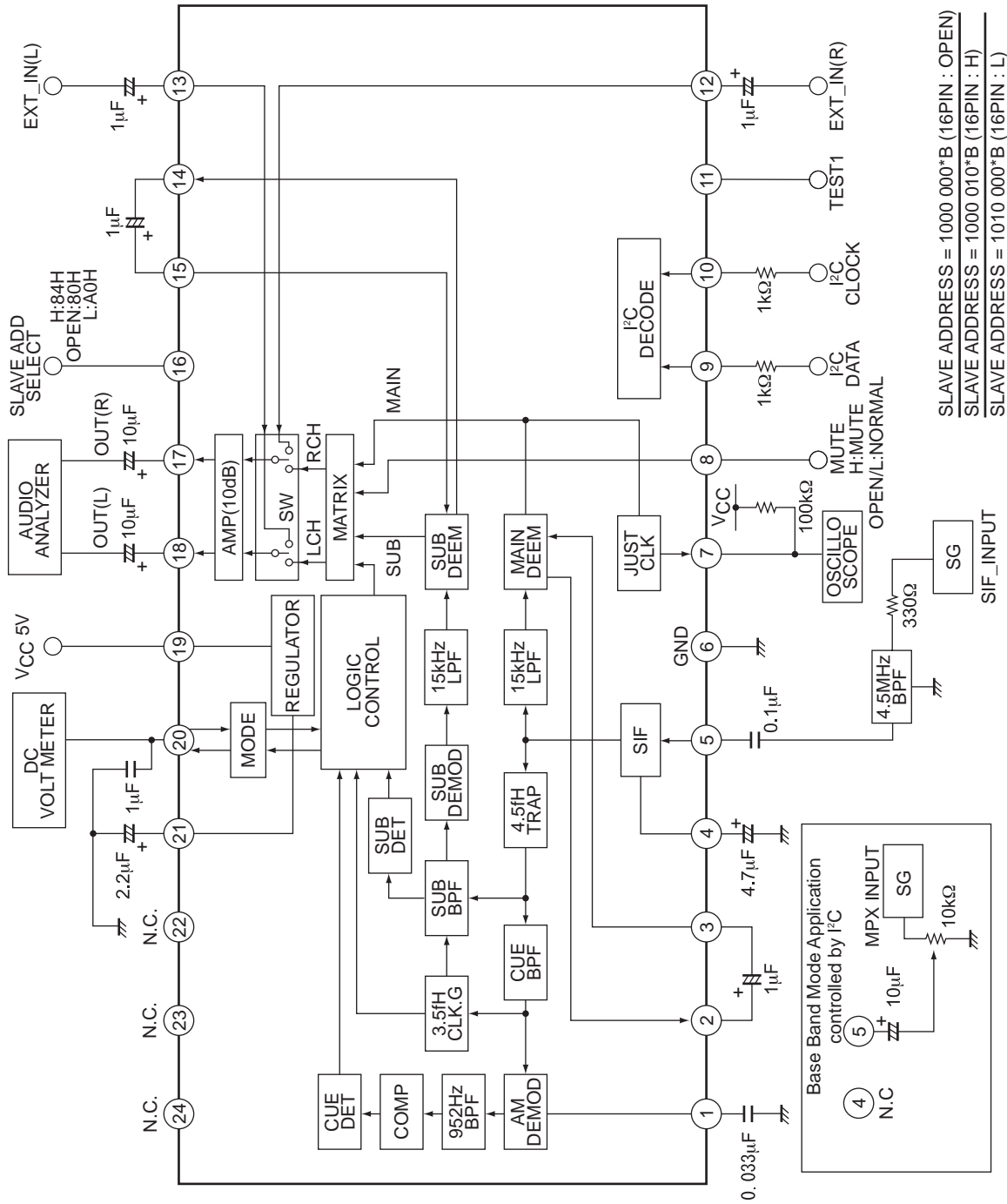
unit : mm (typ)

3175C

[LA72715NV]

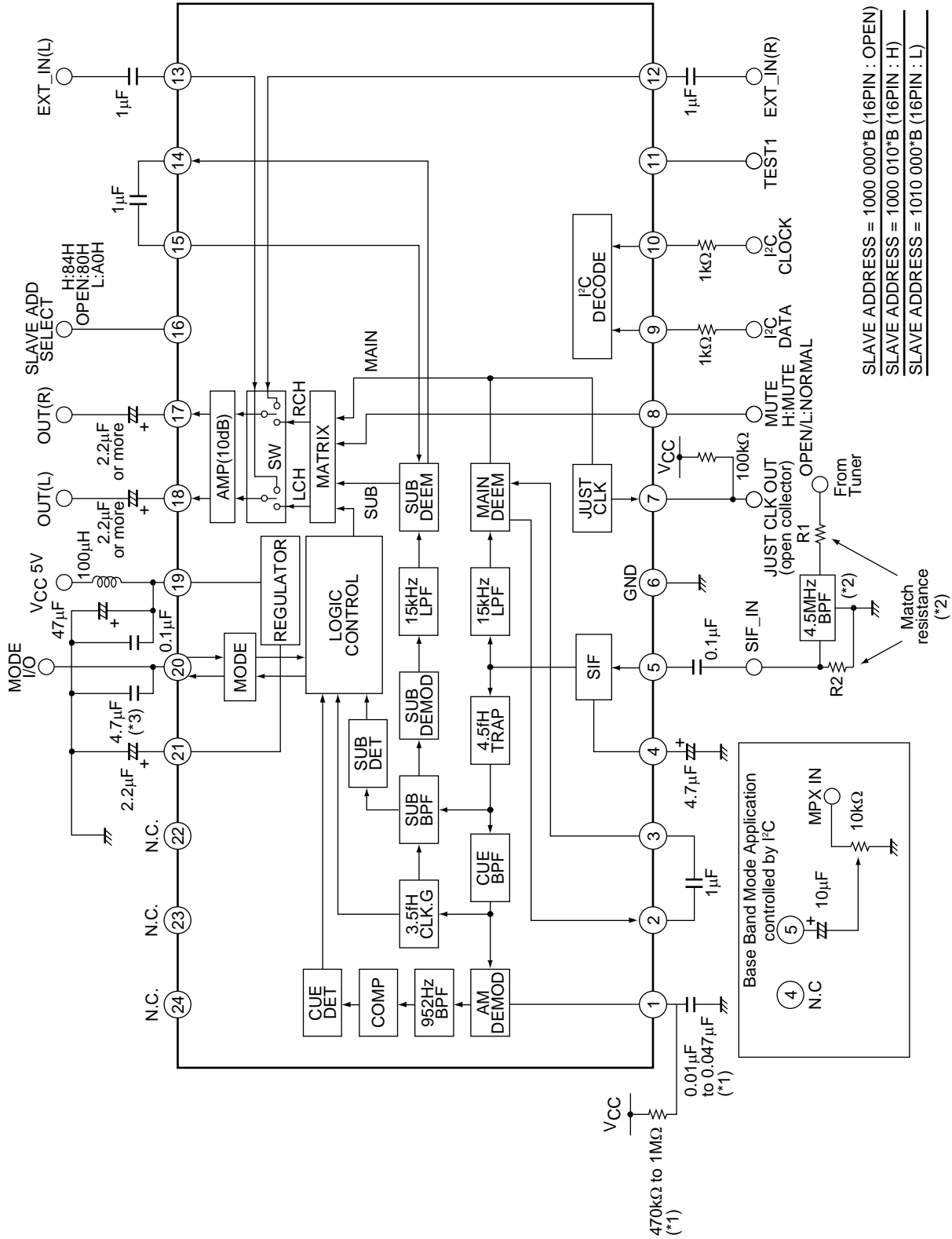


Block Diagram and Test Circuit



SLAVE ADDRESS = 1000 000*B (16PIN : OPEN)
SLAVE ADDRESS = 1000 010*B (16PIN : H)
SLAVE ADDRESS = 1010 000*B (16PIN : L)

Block Diagram and Application Circuit Example



SLAVE ADDRESS = 1000 000*B (16PIN : OPEN)
 SLAVE ADDRESS = 1000 010*B (16PIN : H)
 SLAVE ADDRESS = 1010 000*B (16PIN : L)

The value of (1*), (2*), and (3*) affects sensitivity for signal detection. It must be adjusted depending on the circumstances by the user.

(1*): Recommended constant value $0.0033\mu\text{F} + 470\text{k}\Omega$ (values when tested)

(2*): Recommended matching resistor value $R1=1\text{k}\Omega$, $R2=1\text{k}\Omega$

Recommended BPF Murata SFSRA4M50DF00-B0

(3*): Recommended constant value $4.7\mu\text{F}$ to $10\text{k}\Omega$

The ceramic capacitor may be used for the electrolytic capacitor.

LA72715NV

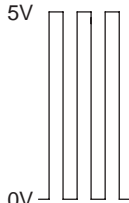
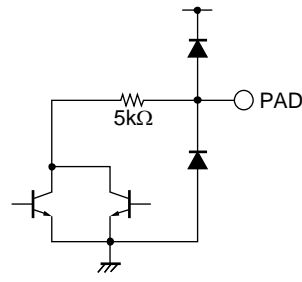
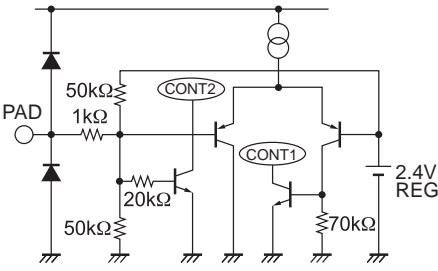
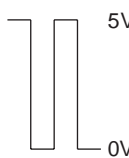
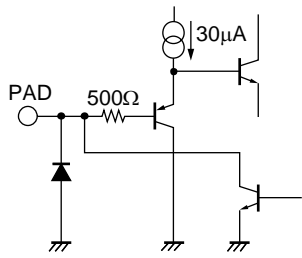
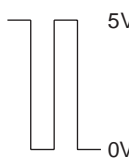
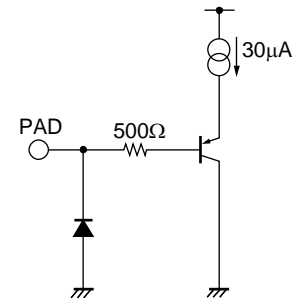
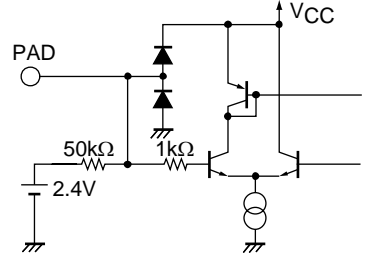
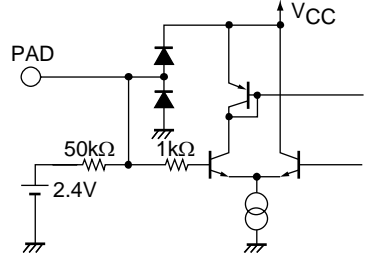
Pin Functions

Pin No.	Pin Name	DC voltage AC level	Function	Equivalent Circuit
1	AM DETECTOR	DC : 2.3V	Reference terminal of AM detection.	
2 14	DC FILTER OUT	2pin DC : 2.6V 14pin DC : 2.1V	Absorbing the DC offset of signal line by external capacity.	
3 15	DC FILTER IN	DC : 2.4V	Absorbing the DC offset of signal line by external capacity.	
4	FM FILTER	DC : 2.9V	Filter terminal for making stable DC voltage of FM detection output in SIF part. Normally, use a condenser of 4.7μF. Increase the capacity value with concerning frequency characteristics of low level.	
5	SIF INPUT	DC : 2.4V	Input terminal for SIF. The input impedance is about 5kΩ. Be care for about pattern layout of the input circuit, because of causing buzz-beat and buzz by leaking noise signal into the input terminal. (The noise signal depending on sound is particularly video signal and chroma signal and so on. VIF carrier becomes noise signal.)	
6	GND			

Continued on next page.

LA72715NV

Continued from preceding page.

Pin No.	Pin Name	DC voltage AC level	Function	Equivalent Circuit
7	JUST CLOCK OUT		Rectangle wave output for JUST CLOCK. (OPEN Collector) 100kΩ Pull-up	
8	MUTE control pin & Distinction control.	DC : 0V	3.0V to V _{CC} : MUTE (CONT 1) OPEN (0.9V) : NORM 0V : NORM & Detection AREA Control (CONT2) Use it within the range of 0 to 0.2V when you operate usually.	
9	Serial data input pin.		High : 2.5V to 5V Low : 0V to 1.5V	
10	Serial CLK input pin		High : 2.5V to 5V Low : 0V to 1.5V	
11	TEST1			
12	EXTIN_R	DC : 2.4V -14.5dBV	EXT input Rch not used : OPEN	
13	EXTIN_L	DC : 2.4V -14.5dBV	EXT input Lch not used : OPEN	

Continued on next page.

LA72715NV

Continued from preceding page.

Pin No.	Pin Name	DC voltage AC level	Function	Equivalent Circuit
16	SLAVE ADD SELECT			
17 18	Line Out (R) terminal Line Out (L) terminal	DC : 2.4V AC : -4.5dBV	Line output pin.	
19	V _{CC} 5V			
20	MTS MODE OUT	No signal DC : 2.0V	Detection output for M.T.S. signal. BILINGUAL :3.0V MONO :2.0V STEREO :1.0V	
21	REG FILT	DC : 2.4V	Filter terminal of reference voltage source	
22 23 24	NC			

I²C BUS Serial Interface Specification

(1) Data Transfer Manual

This LSI adopts control method (I²C-BUS) with serial data, and controlled by two terminals which called SCL (serial clock) and SDA (serial data). At first, set up^{*1} the condition of starting data transfer, and after that, input 8 bit data to SDA terminal with synchronized SCL terminal clock. The order of transferring is first, MSB (the Most Scale of Bit), and save the order. The 9th bit takes ACK (Acknowledge) period, during SCL terminal takes 'H', this LSI pull down the SDA terminal. After transferred the necessary data, two terminals lead to set up and of^{*2} data transfer stop condition, thus the transfer comes to close.

*1 Defined by SCL rise down SDA during 'H' period.

*2 Defined by SCL rise up SDA during 'H' period.

(2) Transfer Data Format

After transfer start condition, transfers slave address (1000 000*) to SDA terminal, control data, then, stop condition (See figure 1).

Slave address is made up of 7bits, ^{*3}8th bit shows the direction of transferring data, if it is 'L' takes write mode (As this LSI side, this is input operation mode), and in case of 'H' reading mode (As this LSI side, this is output operation mode).

Data works with all of bit, transfer the stop condition before stop 8bit transfer, and to stop transfer, it will be canceled the transfer dates. At READ mode, this LSI outputs during ACK period, please must input 9 clocks.

*3 It is called R/W bit.

LA72715NV

Fig.1 DATA STRUCTURE “WRITE” mode

START Condition	Slave Address	R/W L	ACK	Control data	ACK	STOP condition
-----------------	---------------	----------	-----	--------------	-----	----------------

Fig.2 DATA STRUCTURE “READ” mode

START condition	Slave Address	R/W H	ACK	Internal Data *	ACK	STOP condition
-----------------	---------------	----------	-----	-----------------	-----	----------------

* The output data synchronizes with the clock of SCL pin. Then the ACK output is made after the output data.

- bit8 is result of STERO DET (H : STEREO)
- bit7 is result of BILINGUAL DET (H : BILINGUAL)
- bit6 is Initial Condition ‘H’
- bit5 to bit1 are fixed to ‘L’

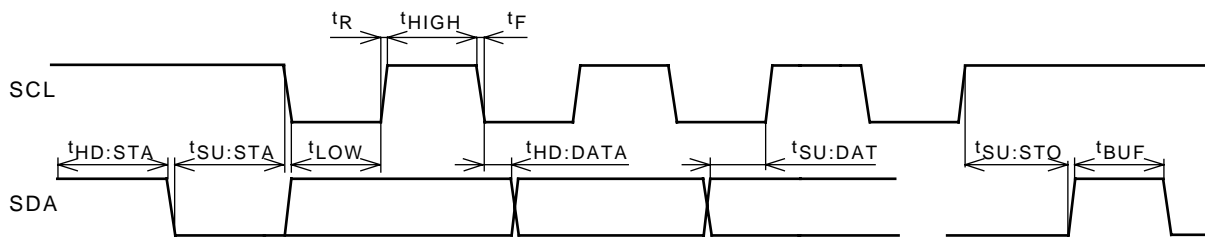
(3) Initialize

This IC is initialized for circuit protection. Initial condition is “01h (Main-mode)”.

Reference

Parameter	Symbol	min	max	unit
LOW level input voltage	V_{IL}	-0.5	1.5	V
HIGH level input voltage	V_{IH}	2.5	5.5	V
LOW level output current	I_{OL}		3.0	mA
SCL clock frequency	f_{SCL}	0	100	kHz
Set-up time for a repeated START condition	$t_{SU : STA}$	4.7		μs
Hold time START condition. After this period, the first clock pulse is generated	$t_{HD : STA}$	4.0		μs
LOW period of the SCL clock	t_{LOW}	4.7		μs
Rise time of both SDA and SDL signals	t_R	0	1.0	μs
HIGH period of the SCL clock	t_{HIGH}	4.0		μs
Fall time of both SDA and SDL signals	t_F	0	1.0	μs
Data hold time	$t_{HD : DAT}$	0		μs
Data set-up time	$t_{SU : DAT}$	250		ns
Set-up time for STOP condition	$t_{SU : STO}$	4.0		μs
BUS free time between a STOP and START condition	t_{BUF}	4.7		μs

Definition of Timing



LA72715NV

I²C Control/LA72715NV Group number is ONLY 1 (Normal Use).

Grp-1

D8	D7	D6	D5	D4	D3	D2	D1	Condition
						0	0	Bilingual
*						0	1	Main
						1	0	Sub
						1	1	(Prohibit)
*					0			Normal
					1			Forced MONO
*				0				Normal (MUTE OFF)
				1				MUTE
*			0					TV Mode (SW Normal)
			1					EXT Mode (SW EXT)
*		0						JUST CLOCK OFF
		1						JUST CLOCK ON
*	0							SIF Mode
	1							BASE BAND Mode
*	0							Fix
	1							Prohibit (TEST Mode)

*: Initial condition

Read out data

D8	D7	D6	D5	D4	D3	D2	D1	Condition
			0	0	0	0	0	Fixed
0								Normal
1								Stereo det
	0							Normal
	1							Bilingual det
		0						Except an initial condition
		1						Initial condition

Test Mode Condition

When STOP condition transform at Grp-1 data-end, controlled NORMAL mode.

Grp-2 (Only test condition : Normally, this group is hidden group)

D8	D7	D6	D5	D4	D3	D2	D1	Condition/Monitor position
0	0	0	0	0	0	0	0	-
0	0	0	0	0	0	0	1	TEST-01 SIF out
0	0	0	0	0	0	1	0	TEST-02 SUB FIL out
0	0	0	0	0	0	1	1	TEST-03 CUE FIL out
0	0	0	0	0	1	0	0	TEST-04 SUD DET out
0	0	0	0	0	1	0	1	TEST-05 CUE DC1 out
0	0	0	0	0	1	1	0	TEST-06 SUB DET2 out
0	0	0	0	0	1	1	1	TEST-07 110K out
0	0	0	0	1	0	0	0	TEST-08 28K out
0	0	0	0	1	0	0	1	TEST-09 CUE PLS out
0	0	0	0	1	0	1	0	TEST-10 FIL ZAP LEVEL

SLAVE ADDRESS 80H (16pin : OPEN)

SLAVE ADDRESS 84H (16pin : V_{CC})

SLAVE ADDRESS A0H (16pin : GND)

LA72715NV

Mode Select (pin & I²C setting)

Broadcast signal	MUTE PIN setting	I ² C					OUTPUT MODE			READ MODE OUT		MODE I/O
	8pin	D5	D4	D3	D2	D1	LCH (18pin)	RCH (17pin)	MODE	D8	D7	20pin
Bilingual	L or OPEN	0	0	0	0	0	MAIN	SUB	BOTH	0	1	3V
	L or OPEN	0	0	0	0	1	MAIN	MAIN	MAIN	0	1	
	L or OPEN	0	0	0	1	0	SUB	SUB	SUB	0	1	
	L or OPEN	0	0	1	*	*	MAIN	MAIN	MONO	0	1	
	*	*	1	*	*	*	MUTE	MUTE	MUTE	0	1	
	H	*	*	*	*	*	MUTE	MUTE	MUTE	0	1	
	L or OPEN	1	0	*	*	*	EXT L	EXT R	EXT	0	1	
STEREO	L or OPEN	0	0	0	*	*	L	R	STEREO	1	0	1V
	L or OPEN	0	0	1	*	*	L+R	L+R	MONO	1	0	
	*	*	1	*	*	*	MUTE	MUTE	MUTE	1	0	
	H	*	*	*	*	*	MUTE	MUTE	MUTE	1	0	
	L or OPEN	1	0	*	*	*	EXT L	EXT R	EXT	1	0	
MONO	L or OPEN	0	0	*	*	*	L+R	L+R	MONO	0	0	2V
	*	*	1	*	*	*	MUTE	MUTE	MUTE	0	0	
	H	*	*	*	*	*	MUTE	MUTE	MUTE	0	0	
	L or OPEN	1	0	*	*	*	EXT L	EXT R	EXT	0	0	

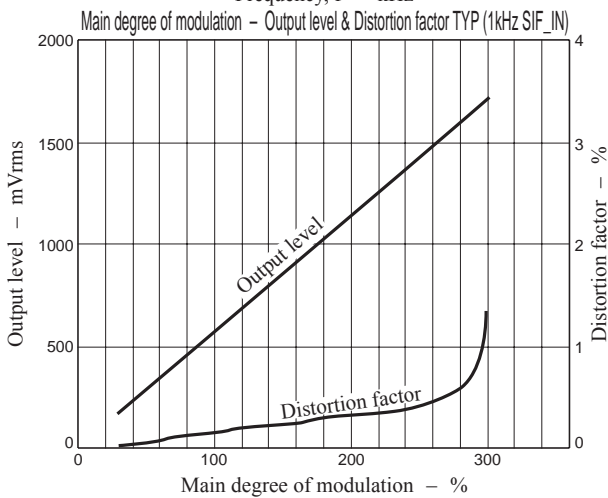
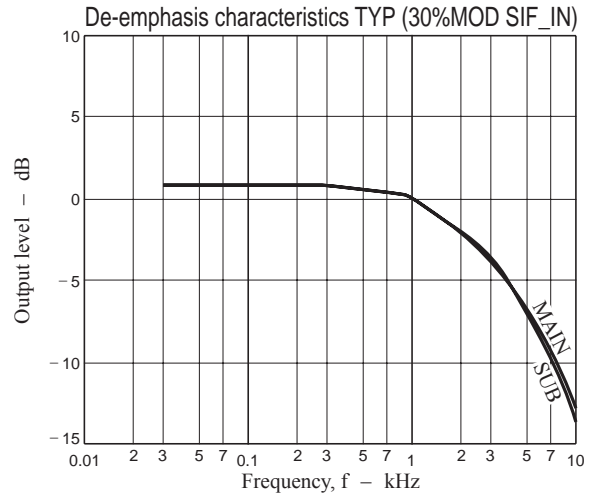
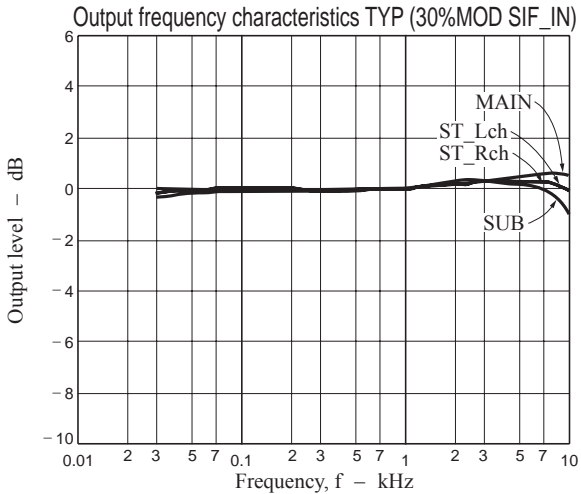
16pin : Slave address select. 0V to 1.5V : A0H, OPEN : 80H, 3.0V to V_{CC} : 84H

Serial Data Specification (I²C bus communication)

Data bit							
MSB D8	D7	D6	D5	D4	D3	D2	LSB D1
TEST	SIF or BASE BAND	JUST CLK	EXT SOURCE SELECT	NORMAL OUT MUTE	Forced MONO	Bilingual mode select	
<u>0</u> : OFF 1 : ON	<u>0</u> : SIF 1 : BASE BAND	<u>0</u> : OFF 1 : ON	<u>0</u> : OFF(TV) 1 : EXT	<u>0</u> : OFF 1 : ON	<u>0</u> : OFF 1 : ON	00: BILINGUAL <u>01</u> : MAIN 10 : SUB 11 : Unusable	

Note : Underline shows default setting

LA72715NV Reference Characteristics



- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of July, 2010. Specifications and information herein are subject to change without notice.