DDR4 SDRAM MiniRDIMM

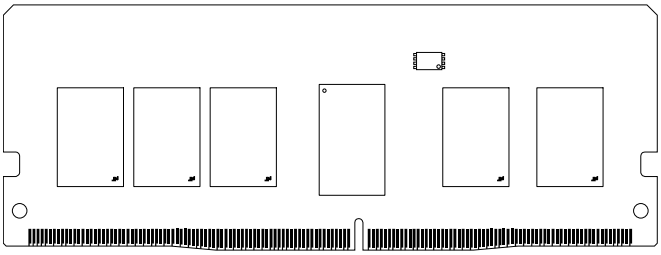
MTA9ASF1G72PKIZ – 8GB

Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin, registered dual in-line mini memory module (MiniRDIMM)
- Fast data transfer rates: PC4-3200, PC4-2666
- 8GB (1 Gig x 72)
- V_{DD} = 1.20V (NOM)
- V_{PP} = 2.5V (NOM)
- V_{DDSPD} = 2.5V (NOM)
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die V_{REFDQ} generation and calibration
- Single-rank
- On-board I^2C temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

Figure 1: 288-Pin MiniRDIMM (MO-314, R/C-ZZ)

Module Height: 30mm (1.181 in)



Options — Marking

- Operating temperature
  - Industrial (–40°C ≤ T_{OPER} ≤ +95°C) — I
- Package
  - 288-pin DIMM (halogen-free) — Z
- Frequency/CAS latency
  - 0.62ns @ CL = 22 (DDR4-3200) — -3G2
  - 0.75ns @ CL = 19 (DDR4-2666) — -2G6

Table 1: Key Timing Parameters

Speed Grade	PC4-	Data Rate (MT/s) CL = 24	22/21	20	19	18	17	16	15	14	13	12	11	10	9	tRCD (ns)	tRP (ns)	tRC (ns)
-3G2	3200	3200	3200/–	2666	2666	2400	2400	2133	2133	1866	1866	1600	1600	1333	–	13.75	13.75	45.75
-2G9	2933	–	2933/2933	2666	2666	2400	2400	2133	2133	1866	1866	1600	1600	1333	–	14.32	14.32	46.32
-2G6	2666	–	–	2666	2666	2400	2400	2133	2133	1866	1866	1600	1600	1333	–	14.16	14.16	46.16
-2G3	2400	–	–	–	–	2400	2400	2133	2133	1866	1866	1600	1600	1333	–	14.16	14.16	46.16

Table 1: Key Timing Parameters (Continued)

Speed Grade	PC4-	Data Rate (MT/s) CL = 24	22/21	20	19	18	17	16	15	14	13	12	11	10	9	^{t}RCD (ns)	^{t}RP (ns)	^{t}RC (ns)
-2G1	2133	–	–	–	–	–	–	2133	2133	1866	1866	1600	1600	1333	1333	13.5	13.5	46.5

Table 2: Addressing

Parameter	8GB
Row address	64K A[15:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	8Gb (1 Gig x 8), 16 banks
Module rank address	1 CS0_n

Table 3: Part Numbers and Timing Parameters – 8GB Modules

Base device: MT40A1G8,[1] 8Gb DDR4 SDRAM

Part Number[2]	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles (^{t}CL-^{t}RCD-^{t}RP)
MTA9ASF1G72PKIZ-3G2__	8GB	1 Gig x 72	25.6 GB/s	0.62ns/3200 MT/s	22-22-22
MTA9ASF1G72PKIZ-2G6__	8GB	1 Gig x 72	21.3 GB/s	0.75ns/2666 MT/s	19-19-19

Notes:
1. The data sheet for the base device can be found on micron.com.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA9ASF1G72PKIZ-3G2E1.

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Pin Assignments

The pin assignment table below is a comprehensive list of all possible pin assignments for DDR4 MiniRDIMM modules. See the Functional Block Diagram for pins specific to this module.

Table 4: Pin Assignments

288-Pin DDR4 MiniRDIMM Front								288-Pin DDR4 MiniRDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	NC	37	V_{SS}	73	A1	109	DQ41	145	V_{REFCA}	181	V_{SS}	217	RFU	253	DQ45
2	NC	38	DQ24	74	V_{DD}	110	V_{SS}	146	NC	182	DQ28	218	V_{DD}	254	V_{SS}
3	RFU	39	V_{SS}	75	CK0_t	111	DQS5_c	147	RFU	183	V_{SS}	219	CK1_t	255	DQS14_t/ DM5_n
4	V_{SS}	40	DQ25	76	CK0_c	112	DQS5_t	148	V_{SS}	184	DQ29	220	CK1_c	256	DQS14_c
5	DQ0	41	V_{SS}	77	V_{DD}	113	V_{SS}	149	DQ4	185	V_{SS}	221	V_{DD}	257	V_{SS}
6	V_{SS}	42	DQS3_c	78	RFU	114	DQ42	150	V_{SS}	186	DQS12_t/ DM3_n	222	RFU	258	DQ46
7	DQ1	43	DQS3_t	79	V_{TT}	115	V_{SS}	151	DQ5	187	DQS12_c	223	V_{TT}	259	V_{SS}
8	V_{SS}	44	V_{SS}	80	EVENT_n	116	DQ43	152	V_{SS}	188	V_{SS}	224	PARITY	260	DQ47
9	DQS0_c	45	DQ26	81	V_{DD}	117	V_{SS}	153	DQS9_t/ DM0_n	189	DQ30	225	V_{DD}	261	V_{SS}
10	DQS0_t	46	V_{SS}	82	A0	118	DQ48	154	DQS9_c	190	V_{SS}	226	BA1	262	DQ52
11	V_{SS}	47	DQ27	83	BA0	119	V_{SS}	155	V_{SS}	191	DQ31	227	A10/ AP	263	V_{SS}
12	DQ2	48	V_{SS}	84	V_{DD}	120	DQ49	156	DQ6	192	V_{SS}	228	V_{DD}	264	DQ53
13	V_{SS}	49	CB0	85	RAS_n/ A16	121	V_{SS}	157	V_{SS}	193	CB4	229	WE_n/ A14	265	V_{SS}
14	DQ3	50	V_{SS}	86	CS0_n	122	DQS6_c	158	DQ7	194	V_{SS}	230	CAS_n/ A15	266	DQS15_t/ DM6_n
15	V_{SS}	51	CB1	87	V_{DD}	123	DQS6_t	159	V_{SS}	195	CB5	231	V_{DD}	267	DQS15_c
16	DQ8	52	V_{SS}	88	ODT0	124	V_{SS}	160	DQ12	196	V_{SS}	232	A13	268	V_{SS}
17	V_{SS}	53	DQS8_c	89	CS1_n/ NC	125	DQ50	161	V_{SS}	197	DQS17_t/ DM8_n	233	A17/ NC	269	DQ54
18	DQ9	54	DQS8_t	90	V_{DD}	126	V_{SS}	162	DQ13	198	DQS17_c	234	V_{DD}	270	V_{SS}
19	V_{SS}	55	V_{SS}	91	ODT1/ NC	127	DQ51	163	V_{SS}	199	V_{SS}	235	NC/CS3_n/ C1	271	DQ55
20	DQS1_c	56	CB2	92	CS2_n/C0/ NC	128	V_{SS}	164	DQS10_t/ DM1_n	200	CB6	236	NC/ C2	272	V_{SS}
21	DQS1_t	57	V_{SS}	93	V_{DD}	129	DQ56	165	DQS10_c	201	V_{SS}	237	V_{DD}	273	DQ60
22	V_{SS}	58	CB3	94	RFU	130	V_{SS}	166	V_{SS}	202	CB7	238	RFU	274	V_{SS}
23	DQ10	59	V_{SS}	95	V_{SS}	131	DQ57	167	DQ14	203	V_{SS}	239	V_{SS}	275	DQ61
24	V_{SS}	60	ALERT_n	96	DQ32	132	V_{SS}	168	V_{SS}	204	RESET_n	240	DQ36	276	V_{SS}
25	DQ11	61	CKE0	97	V_{SS}	133	DQS7_c	169	DQ15	205	RFU	241	V_{SS}	277	DQS16_t/ DM7_n
26	V_{SS}	62	V_{DD}	98	DQ33	134	DQS7_t	170	V_{SS}	206	V_{DD}	242	DQ37	278	DQS16_c
27	DQ16	63	ACT_n	99	V_{SS}	135	V_{SS}	171	DQ20	207	CKE1/ NC	243	V_{SS}	279	V_{SS}
28	V_{SS}	64	BG0	100	DQS4_c	136	DQ58	172	V_{SS}	208	BG1	244	DQS13_t/ DM4_n	280	DQ62
29	DQ17	65	V_{DD}	101	DQS4_t	137	V_{SS}	173	DQ21	209	V_{DD}	245	DQS13_c	281	V_{SS}

Table 4: Pin Assignments (Continued)

288-Pin DDR4 MiniRDIMM Front								288-Pin DDR4 MiniRDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
30	V_{SS}	66	A12/BC_n	102	V_{SS}	138	DQ59	174	V_{SS}	210	A11	246	V_{SS}	282	DQ63
31	DQS2_c	67	A9	103	DQ34	139	V_{SS}	175	DQS11_t/ DM2_n	211	A7	247	DQ38	283	V_{SS}
32	DQS2_t	68	V_{DD}	104	V_{SS}	140	SA0	176	DQS11_c	212	V_{DD}	248	V_{SS}	284	SA1
33	V_{SS}	69	A8	105	DQ35	141	V_{DDSPD}	177	V_{SS}	213	A5	249	DQ39	285	SA2
34	DQ18	70	A6	106	V_{SS}	142	SDA	178	DQ22	214	A4	250	V_{SS}	286	SCL
35	V_{SS}	71	V_{DD}	107	DQ40	143	V_{PP}	179	V_{SS}	215	V_{DD}	251	DQ44	287	V_{PP}
36	DQ19	72	A3	108	V_{SS}	144	V_{PP}	180	DQ23	216	A2	252	V_{SS}	288	V_{PP}

Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 modules. All pins listed may not be supported on this module. See Functional Block Diagram for pins specific to this module.

Table 5: Pin Descriptions

Symbol	Type	Description
Ax	Input	**Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM.
A10/AP	Input	**Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses.
A12/BC_n	Input	**Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH = no burst chop; LOW = burst chopped). See Command Truth Table in the DDR4 component data sheet.
ACT_n	Input	**Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table.
BAx	Input	**Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command.
BGx	Input	**Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0.
C0, C1, C2 (RDIMM/LRDIMM only)	Input	**Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code.
CKx_t CKx_c	Input	**Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c.
CKEx	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After V_{REFCA} has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh.
CSx_n	Input	**Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code (CS2_n and CS3_n are not used on UDIMMs).

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
ODTx	Input	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT (R_{TT}) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, R_{TT} is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable R_{TT}.
PARITY	Input	**Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW.
RAS_n/A16 CAS_n/A15 WE_n/A14	Input	**Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table.
RESET_n	CMOS Input	**Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation.
SAx	Input	**Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the I^2C bus.
SCL	Input	**Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I^2C bus.
DQx, CBx	I/O	**Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal V_{REF} level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled.
DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIl_n)	I/O	**Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs).
SDA	I/O	**Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device.
DQS_t DQS_c DQSU_t DQSU_c DQSL_t DQSL_c	I/O	**Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe.
ALERT_n	Output	**Alert output:** Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT_n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT_n goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT_n pin must be connected to V_{DD} on DIMMs.
EVENT_n	Output	**Temperature event:** The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors.

Table 5: Pin Descriptions (Continued)

Symbol	Type	Description
TDQS_t TDQS_c (x8 DRAM-based RDIMM only)	Output	**Termination data strobe:** When enabled via the mode register, the DRAM device enables the same R_{TT} termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component data sheet (TDQS_t and TDQS_c are not valid for UDIMMs).
V_{DD}	Supply	**Module power supply:** 1.2V (TYP).
V_{PP}	Supply	**DRAM activating power supply:** 2.5V –0.125V / +0.250V.
V_{REFCA}	Supply	Reference voltage for control, command, and address pins.
V_{SS}	Supply	Ground.
V_{TT}	Supply	Power supply for termination of address, command, and control $V_{DD}/2$.
V_{DDSPD}	Supply	Power supply used to power the I^2C bus for SPD.
RFU	–	Reserved for future use.
NC	–	**No connect:** No internal electrical connection is present.
NF	–	**No function:** May have internal connection present, but has no function.

DQ Map

Table 6: Component-to-Module DQ Map

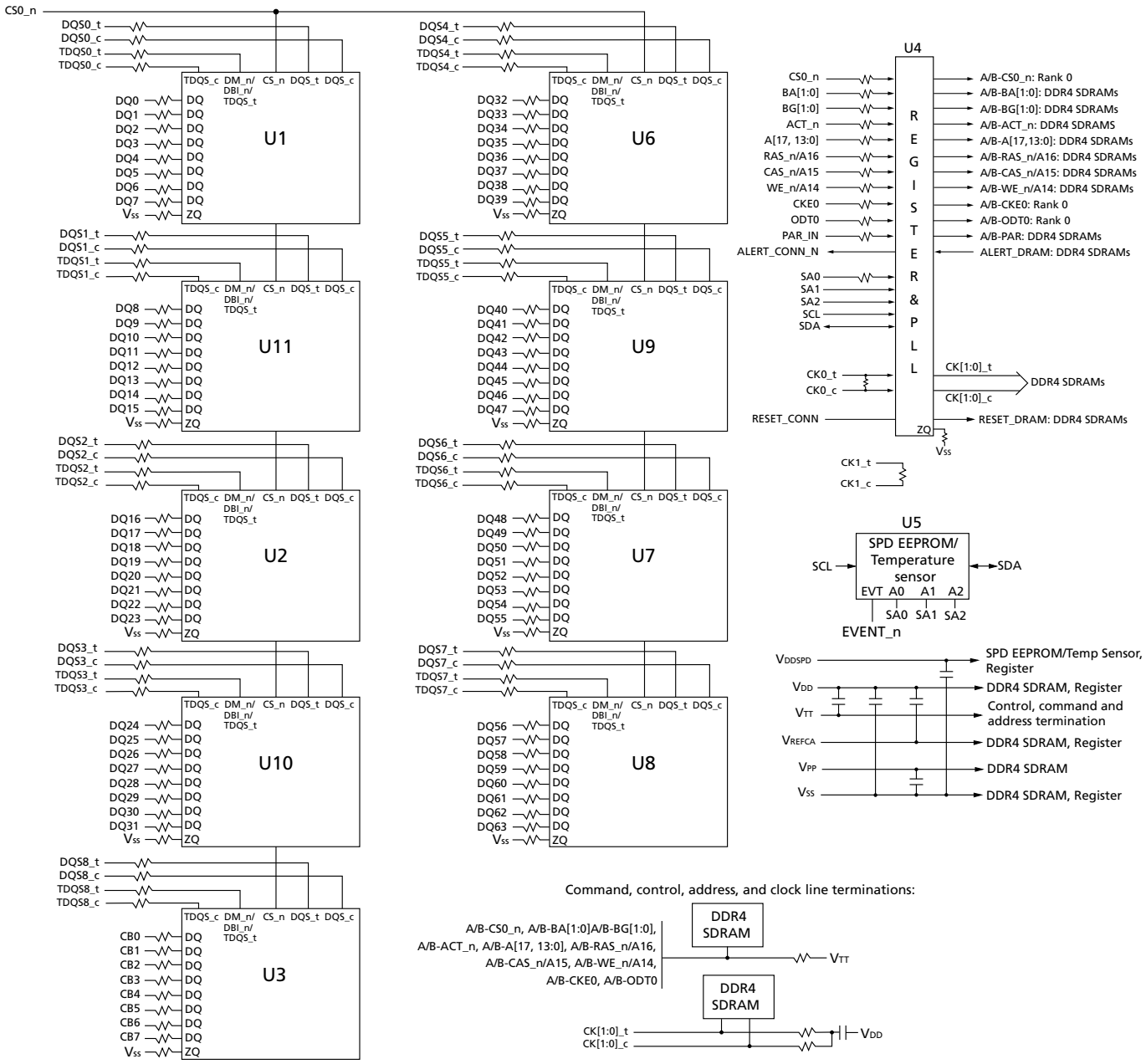
Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	3	14	U2	0	19	36
	1	1	7		1	16	27
	2	2	12		2	18	34
	3	0	5		3	17	29
	4	7	158		4	23	180
	5	4	149		5	20	171
	6	6	156		6	22	178
	7	2	151		7	21	173
U3	0	CB3	58	U6	0	38	247
	1	CB0	49		1	37	242
	2	CB2	56		2	39	249
	3	CB1	51		3	36	240
	4	CB7	202		4	35	105
	5	CB4	193		5	33	98
	6	CB6	200		6	34	103
	7	CB5	195		7	32	96
U7	0	54	269	U8	0	56	129
	1	53	264		1	58	136
	2	55	271		2	57	131
	3	52	262		3	59	138
	4	50	125		4	60	273
	5	48	118		5	63	282
	6	51	127		6	61	275
	7	49	120		7	62	280
U9	0	41	109	U10	0	29	184
	1	42	114		1	30	189
	2	40	107		2	28	182
	3	43	116		3	31	191
	4	44	251		4	24	38
	5	47	260		5	27	47
	6	45	251		6	25	40
	7	46	258		7	26	45

Table 6: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	9	18				
	1	10	23				
	2	8	16				
	3	11	25				
	4	12	160				
	5	15	169				
	6	13	162				
	7	14	167				

Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with two or four internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM devices have four internal bank groups consisting of four memory banks each, providing a total of 16 banks. 16-bit-wide DDR4 SDRAM devices have two internal bank groups consisting of four memory banks each, providing a total of eight banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single 8*n*-bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR4 modules use two sets of differential signals: DQS_t and DQS_c to capture data and CK_t and CK_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

Fly-By Topology

DDR4 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR4.

Module Manufacturing Location

Micron Technology manufactures modules at sites world-wide. Customers may receive modules from any of the following manufacturing locations:

Table 7: DRAM Module Manufacturing Locations

Manufacturing Site Location	Country of Origin Specified on Label
Boise, USA	USA
Aguadilla, Puerto Rico	Puerto Rico
Xian, China	China
Singapore	Singapore

Address Mapping to DRAM

Address Mirroring

To achieve optimum routing of the address bus on DDR4 multi rank modules, the address bus will be wired as shown in the table below, or mirrored. For quad rank modules, ranks 1 and 3 are mirrored and ranks 0 and 2 are non-mirrored. Highlighted address pins have no secondary functions allowing for normal operation when cross-wired. Data is still read from the same address it was written. However, Load Mode operations require a specific address. This requires the controller to accommodate for a rank that is "mirrored." Systems may reference DDR4 SPD to determine if the module has mirroring implemented or not. See the JEDEC DDR4 SPD specification for more details.

Table 8: Address Mirroring

Edge Connector Pin	DRAM Pin, Non-mirrored	DRAM Pin, Mirrored
A0	A0	A0
A1	A1	A1
A2	A2	A2
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
A9	A9	A9
A10	A10	A10
A11	A11	A13
A13	A13	A11
A12	A12	A12
A14	A14	A14
A15	A15	A15
A16	A16	A16
A17	A17	A17
BA0	BA0	BA1
BA1	BA1	BA0
BG0	BG0	BG1
BG1	BG1	BG0

Registering Clock Driver Operation

Registered DDR4 SDRAM modules use a registering clock driver device consisting of a register and a phase-lock loop (PLL). The device complies with the JEDEC DDR4 RCD specification.

To reduce the electrical load on the host memory controller's command, address, and control bus, Micron's RDIMMs utilize a DDR4 registering clock driver (RCD). The RCD presents a single load to the controller while redriving signals to the DDR4 SDRAM devices, which helps enable higher densities and increase signal integrity. The RCD also provides a low-jitter, low-skew PLL that redistributes a differential clock pair to multiple differential pairs of clock outputs.

Control Words

The RCD device(s) used on DDR4 RDIMMs, LRDIMMs, and NVDIMMs contain configuration registers known as control words, which the host uses to configure the RCD based on criteria determined by the module design. Control words can be set by the host controller through either the DRAM address and control bus or the I^2C bus interface. The RCD I^2C bus interface resides on the same I^2C bus interface as the module temperature sensor and EEPROM.

Parity Operations

The RCD includes a parity-checking function that can be enabled or disabled in control word RC0E. The RCD receives a parity bit at the DPAR input from the memory controller and compares it with the data received on the qualified command and address inputs; it indicates on its open-drain ALERT_n pin whether a parity error has occurred. If parity checking is enabled, the RCD forwards commands to the SDRAM when no parity error has occurred. If the parity error function is disabled, the RCD forwards sampled commands to the SDRAM regardless of whether a parity error has occurred. Parity is also checked during control word WRITE operations unless parity checking is disabled.

Rank Addressing

The chip select pins (CS_n) on Micron's modules are used to select a specific rank of DRAM. The RDIMM is capable of selecting ranks in one of three different operating modes, dependant on setting DA[1:0] bits in the DIMM configuration control word located within the RCD. Direct DualCS mode is utilized for single- or dual-rank modules. For quad-rank modules, either direct or encoded QuadCS mode is used.

Temperature Sensor with SPD EEPROM Operation

Thermal Sensor Operations

The integrated thermal sensor continuously monitors the temperature of the module PCB directly below the device and updates the temperature data register. Temperature data may be read from the bus host at any time, which provides the host real-time feedback of the module's temperature. Multiple programmable and read-only temperature registers can be used to create a custom temperature-sensing solution based on system requirements and JEDEC JC-42.2.

EVENT_n Pin

The temperature sensor also adds the EVENT_n pin (open-drain), which requires a pull-up to V_{DDSPD}. EVENT_n is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration registers. EVENT_n is not used by the serial presence-detect (SPD) EEPROM.

EVENT_n has three defined modes of operation: interrupt, comparator, and TCRIT. In interrupt mode, the EVENT_n pin remains asserted until it is released by writing a 1 to the clear event bit in the status register. In comparator mode, the EVENT_n pin clears itself when the error condition is removed. Comparator mode is always used when the temperature is compared against the TCRIT limit. In TCRIT only mode, the EVENT_n pin is only asserted if the measured temperature exceeds the TCRIT limit; it then remains asserted until the temperature drops below the TCRIT limit minus the TCRIT hysteresis.

SPD EEPROM Operation

DDR4 SDRAM modules incorporate SPD. The SPD data is stored in a 512-byte, JEDEC JC-42.4-compliant EEPROM that is segregated into four 128-byte, write-protectable blocks. The SPD content is aligned with these blocks as shown in the table below.

Block	Range		Description
0	0–127	000h–07Fh	Configuration and DRAM parameters
1	128–255	080h–0FFh	Module parameters
2	256–319	100h–13Fh	Reserved (all bytes coded as 00h)
	320–383	140h–17Fh	Manufacturing information
3	384–511	180h–1FFh	End-user programmable

The first 384 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR4 SDRAM Modules." The remaining 128 bytes of storage are available for use by the customer.

The EEPROM resides on a two-wire I^2C serial interface and is not integrated with the memory bus in any manner. It operates as a slave device in the I^2C bus protocol, with all operations synchronized by the serial clock. Transfer rates of up to 1 MHz are achievable at 2.5V (NOM).

Micron implements reversible software write protection on DDR4 SDRAM-based modules. This prevents the lower 384 bytes (bytes 0 to 383) from being inadvertently programmed or corrupted. The upper 128 bytes remain available for customer use and are unprotected.

Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

Table 9: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DD}	V_{DD} supply voltage relative to V_{SS}	–0.4	1.5	V	1
V_{DDQ}	V_{DDQ} supply voltage relative to V_{SS}	–0.4	1.5	V	1
V_{PP}	Voltage on V_{PP} pin relative to V_{SS}	–0.4	3.0	V	2
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	–0.4	1.5	V	

Table 10: Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	V_{DD} supply voltage	1.14	1.20	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltage – command/address bus	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V	3
I_{VTT}	Termination reference current from V_{TT}	–750	–	750	mA	
V_{TT}	Termination reference voltage (DC) – command/address bus	0.49 × V_{DD} - 20mV	0.5 × V_{DD}	0.51 × V_{DD} + 20mV	V	4
I_{IN}	Input leakage current; any input excluding ZQ; 0V < V_{IN} < 1.1V	–2	–	2	µA	5
I_{ZQ}	Input leakage current; ZQ	–3	–	3	µA	6, 7
$I_{I/O}$	DQ leakage; 0V < V_{IN} < V_{DD}	–4	–	4	µA	7
I_{OZpd}	Output leakage current; V_{OUT} = V_{DD}; DQ is disabled	–	–	5	µA	
I_{OZpu}	Output leakage current; V_{OUT} = V_{SS}; DQ and ODT are disabled; ODT is disabled with ODT input HIGH	–	–	50	µA	
I_{VREFCA}	V_{REFCA} leakage; V_{REFCA} = V_{DD}/2 (after DRAM is initialized)	–2	–	2	µA	7

Notes:
1. V_{DDQ} balls on DRAM are tied to V_{DD}.
2. V_{PP} must be greater than or equal to V_{DD} at all times.
3. V_{REFCA} must not be greater than 0.6 × V_{DD}. When V_{DD} is less than 500mV, V_{REF} may be less than or equal to 300mV.
4. V_{TT} termination voltages in excess of specification limit adversely affect command and address signals' voltage margins and reduce timing margins.
5. Command and address inputs are terminated to V_{DD}/2 in the registering clock driver. Input current is dependent on termination resistance set in the registering clock driver.
6. Tied to ground. Not connected to edge connector.
7. Multiply by number of DRAM die on module.

Table 11: Thermal Characteristics

Symbol	Parameter/Condition	Value	Units	Notes
T_C	Industrial operating case temperature	–40 to 85	°C	1, 2, 3
		>85 to 95	°C	1, 2, 3, 4
T_{OPER}	Normal operating temperature range	0 to 85	°C	5, 6, 7
	Extended temperature operating range (optional)	>85 to 95	°C	5, 7
T_{STG}	Non-operating storage temperature	–55 to 100	°C	8
RH_{STG}	Non-operating storage relative humidity (noncondensing)	5 to 95	%	
N/A	Change rate of storage temperature	20	°C/hour	

Notes:
1. Maximum operating case temperature; T_C is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_C during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_C during operation.
4. If T_C exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.
5. The refresh rate must double when 85°C < T_{OPER} ≤ 95°C.
6. The normal temperature range specifies the temperatures at which all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0°C to 85°C under all operating conditions for the commercial offering; The industrial temperature offering allows the case temperature to go below 0°C to -40°C.
7. For additional information, refer to technical note TN-00-08: "Thermal Applications" available at micron.com.
8. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR4 component data sheets. Component specifications are available at micron.com. Module speed grades correlate with component speed grades, as shown below.

Table 12: Module and Component Speed Grades

DDR4 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Module Speed Grade	Component Speed Grade
-3G2	-062E
-2G9	-068
-2G6	-075
-2G3	-083
-2G1	-093E

Design Considerations

Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

Power

Operating voltages are specified at the edge connector of the module, not at the DRAM. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

I_{DD} Specifications

Table 13: DDR4 I_{DD} Specifications and Conditions – 8GB (Die Revision B)

Values are for the MT40A1G8 DDR4 SDRAM only and are computed from values specified in the 8Gb (1 Gig x 8) component data sheet

Parameter	Symbol	2666	Units
One bank ACTIVATE-PRECHARGE current	I_{DD0}	459	mA
One bank ACTIVATE-PRECHARGE, word line boost, I_{PP} current	I_{PP0}	27	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{DD1}	567	mA
Precharge standby current	I_{DD2N}	315	mA
Precharge standby ODT current	I_{DD2NT}	450	mA
Precharge power-down current	I_{DD2P}	225	mA
Precharge quiet standby current	I_{DD2Q}	270	mA
Active standby current	I_{DD3N}	414	mA
Active standby I_{PP} current	I_{PP3N}	27	mA
Active power-down current	I_{DD3P}	351	mA
Burst read current	I_{DD4R}	1314	mA
Burst write current	I_{DD4W}	1188	mA
Burst refresh current (1 x REF)	I_{DD5R}	504	mA
Burst refresh I_{PP} current (1 x REF)	I_{PP5R}	45	mA
Self refresh current: Normal temperature range (0°C to +85°C)	I_{DD6N}	270	mA
Self refresh current: Extended temperature range (0°C to +95°C)	I_{DD6E}	315	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	I_{DD6R}	180	mA
Auto self refresh current (25°C)	I_{DD6A}	77.4	mA
Auto self refresh current (45°C)	I_{DD6A}	180	mA
Auto self refresh current (75°C)	I_{DD6A}	270	mA
Auto self refresh I_{PP} current	I_{PP6X}	45	mA
Bank interleave read current	I_{DD7}	1620	mA
Bank interleave read I_{PP} current	I_{PP7}	135	mA
Maximum power-down current	I_{DD8}	225	mA

Table 14: DDR4 I_{DD} Specifications and Conditions – 8GB (Die Revision E)

Values are for the MT40A1G8 DDR4 SDRAM only and are computed from values specified in the 8Gb (1 Gig x 8) component data sheet

Parameter	Symbol	3200	Units
One bank ACTIVATE-PRECHARGE current	I_{DD0}	513	mA
One bank ACTIVATE-PRECHARGE, word line boost, I_{PP} current	I_{PP0}	27	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{DD1}	621	mA
Precharge standby current	I_{DD2N}	333	mA
Precharge standby ODT current	I_{DD2NT}	540	mA
Precharge power-down current	I_{DD2P}	225	mA
Precharge quiet standby current	I_{DD2Q}	270	mA
Active standby current	I_{DD3N}	504	mA
Active standby I_{PP} current	I_{PP3N}	27	mA
Active power-down current	I_{DD3P}	387	mA
Burst read current	I_{DD4R}	1512	mA
Burst write current	I_{DD4W}	1395	mA
Burst refresh current (1 x REF)	I_{DD5R}	594	mA
Burst refresh I_{PP} current (1 x REF)	I_{PP5R}	45	mA
Self refresh current: Normal temperature range (0°C to +85°C)	I_{DD6N}	279	mA
Self refresh current: Extended temperature range (0°C to +95°C)	I_{DD6E}	324	mA
Self refresh current: Reduced temperature range (0°C to +45°C)	I_{DD6R}	189	mA
Auto self refresh current (25°C)	I_{DD6A}	77.4	mA
Auto self refresh current (45°C)	I_{DD6A}	189	mA
Auto self refresh current (75°C)	I_{DD6A}	279	mA
Auto self refresh I_{PP} current	I_{PP6X}	45	mA
Bank interleave read current	I_{DD7}	1710	mA
Bank interleave read I_{PP} current	I_{PP7}	135	mA
Maximum power-down current	I_{DD8}	225	mA

Registering Clock Driver Specifications

Table 15: Registering Clock Driver Electrical Characteristics

DDR4 RCD01 devices or equivalent

Parameter	Symbol	Pins	Min	Nom	Max	Units
DC supply voltage	V_{DD}	–	1.14	1.2	1.26	V
DC reference voltage	V_{REF}	V_{REFCA}	0.49 × V_{DD}	0.5 × V_{DD}	0.51 × V_{DD}	V
DC termination voltage	V_{TT}	–	V_{REF} - 40mV	V_{REF}	V_{REF} + 40mV	V
High-level input voltage	$V_{IH.\ CMOS}$	DRST_n	0.65 × V_{DD}	–	V_{DD}	V
Low-level input voltage	$V_{IL.\ CMOS}$		0	–	0.35 × V_{DD}	V
DRST_n pulse width	^{t}IN-IT_Pow-er_stable	–	1.0	–	–	µs
AC high-level output voltage	$V_{OH(AC)}$	All outputs except ALERT_n	V_{TT} + (0.15 × V_{DD})	–	–	V
AC low-level output voltage	$V_{OL(AC)}$		–	–	V_{TT} + (0.15 × V_{DD})	V
AC differential output high measurement level (for output slew rate)	$V_{OHdiff(AC)}$	Yn_t - Yn_c, BCK_t - BCK_c	–	0.3 × V_{DD}	–	mV
AC differential output low measurement level (for output slew rate)	$V_{OLdiff(AC)}$		–	–0.3 × V_{DD}	–	mV

Note: 1. Timing and switching specifications for the register listed are critical for proper operation of DDR4 SDRAM RDIMMs. These are meant to be a subset of the parameters for the specific device used on the module. See the JEDEC RCD01 specification for complete operating electrical characteristics. Registering clock driver parametric values are specified for device default control word settings, unless otherwise stated. The RC0A control word setting does not affect parametric values.

SPD EEPROM Operating Conditions

For the latest SPD data, refer to Micron's SPD page: micron.com/spd.

Table 16: SPD EEPROM DC Operating Conditions

Parameter/Condition	Symbol	Min	Nom	Max	Units
Supply voltage	V_{DDSPD}	–	2.5	–	V
Input low voltage: logic 0; all inputs	V_{IL}	–0.5	–	V_{DDSPD} × 0.3	V
Input high voltage: logic 1; all inputs	V_{IH}	V_{DDSPD} × 0.7	–	V_{DDSPD} + 0.5	V
Output low voltage: 3mA sink current V_{DDSPD} > 2V	V_{OL}	–	–	0.4	V
Input leakage current: (SCL, SDA) V_{IN} = V_{DDSPD} or V_{SSSPD}	I_{LI}	–	–	±5	µA
Output leakage current: V_{OUT} = V_{DDSPD} or V_{SSSPD}, SDA in High-Z	I_{LO}	–	–	±5	µA

Notes:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.
2. All voltages referenced to V_{DDSPD}.

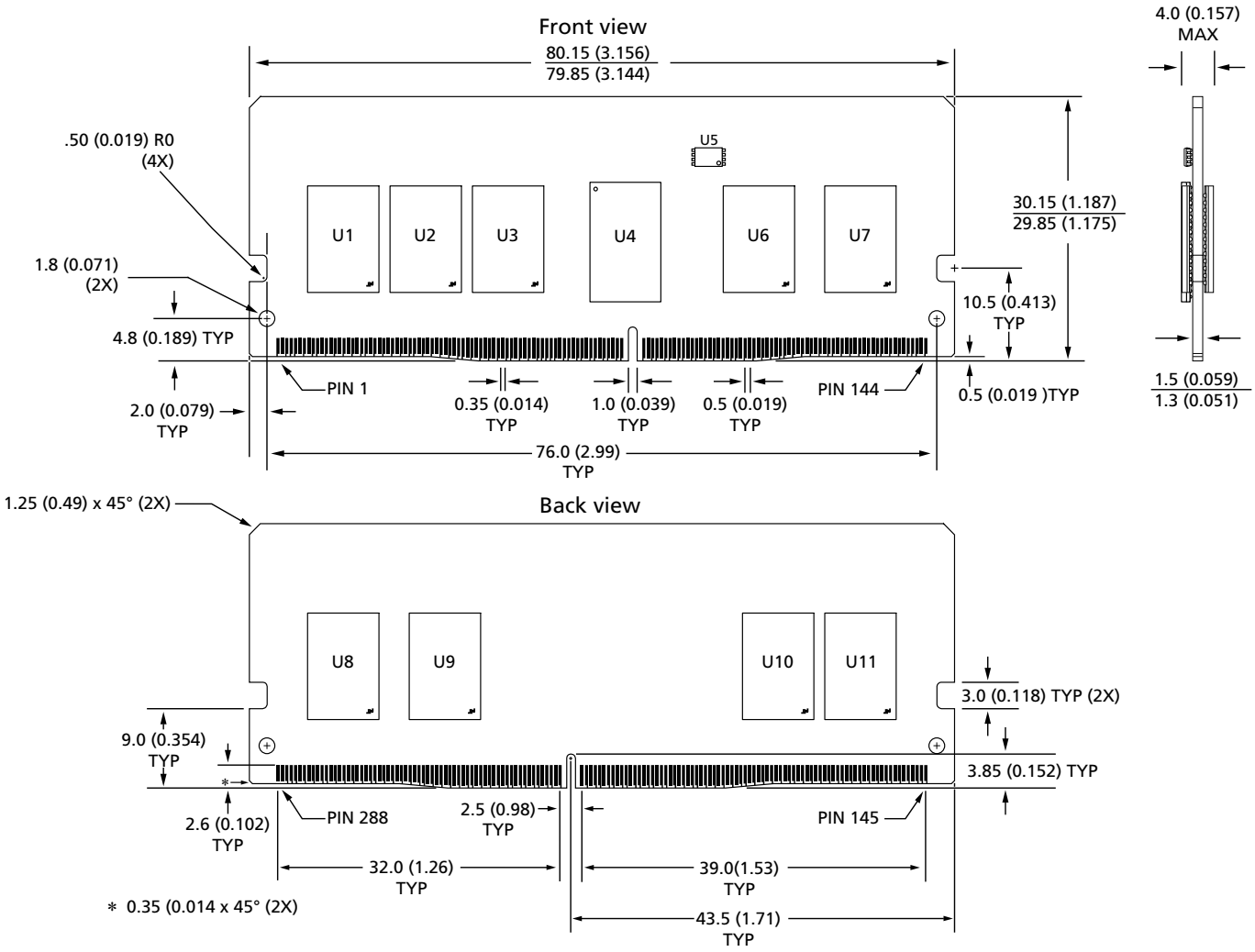
Table 17: SPD EEPROM AC Operating Conditions

Parameter/Condition	Symbol	Min	Max	Units
Clock frequency	^{t}SCL	10	1000	kHz
Clock pulse width HIGH time	^{t}HIGH	260	–	ns
Clock pulse width LOW time	^{t}LOW	500	–	ns
Detect clock LOW timeout	^{t}TIMEOUT	25	35	ms
SDA rise time	^{t}R	–	120	ns
SDA fall time	^{t}F	–	120	ns
Data-in setup time	^{t}SU:DAT	50	–	ns
Data-in hold time	^{t}HD:DI	0	–	ns
Data out hold time	^{t}HD:DAT	0	350	ns
Start condition setup time	^{t}SU:STA	260	–	ns
Start condition hold time	^{t}HD:STA	260	–	ns
Stop condition setup time	^{t}SU:STO	260	–	ns
Time the bus must be free before a new transition can start	^{t}BUF	500	–	ns
Write time	^{t}W	–	5	ms
Warm power cycle time off	^{t}POFF	1	–	ms
Time from power on to first command	^{t}INIT	10	–	ms

Note:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.

Module Dimensions

Figure 3: 288-Pin DDR4 MiniRDIMM



Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.